64-6

INTERIM REPORT

Contract No. FAA/ARDS-444

TASK 2: LABORATORY EVALUATION OF BREADBOARD EQUIPMENT

EXPERIMENTAL EVALUATION OF COMPATIBLE PWI/CAS INTERROGATOR-TRANSPONDER TECHNIQUES

VOLUME 2 OF 2

September 1963

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AVIATION RESEARCH AND DEVELOPMENT SERVICE
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WASHINGTON 25, D.C.

By

SPERRY GYROSCOPE COMPANY
DIVISION OF SPERRY RAND CORPORATION
GREAT NECK, NEW YORK

Sperry Report No. EB-5261-0341-2

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This report has been prepared by Sperry Gyroscope Company Division of Sperry Rand Corporation for the Aviation Research and Development Service, Federal Aviation Agency, under Contract No. FAA/ARDS-444. The contents of this report reflect the views of the contractor, who is responsible for the facts and the accuracy of the data presented herein, and do not necessarily reflect the official views or policy of the FAA.

By

SPERRY GYROSCOPE COMPANY

DIVISION OF SPERRY RAND CORPORATION

GREAT NECK, NEW YORK

Sperry Report No. EB-5261-0341-2

Copy No. 1

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SECTION V

BREADBOARD IMPLEMENTATION

A. DESCRIPTION

This section contains descriptions of the components which make up the CAS and PWI interrogators and the transponder equipment. The components consist of coders, decoders, and computers. Six sections are included, each one corresponding to a particular system component. The operation of the coding and decoding units is described with the aid of detailed block diagrams (figure 5-1 thru 5-4) where the blocks represent standard video and logic circuits. The operation of the computing units is described with the aid of signal schematics (figures 5-5 and 5-6) considered more appropriate for describing the flow of analog data. These block diagrams and signal schematics are contained at the end of this volume. They are followed by other interconnection information in the form of

- interconnection diagrams for the coders and decoders (figures 5-7 through 5-10)
- power schematics and schematics of chassis-mounted transformers for the computing units, which have self-contained power supplies (figures 5-11 through 5-15).

Following the interconnection information are schematic diagrams of the components which comprise these major units (figures 5-16 through 5-62). Component diagrams are identified by the same titles and numeric or alpha-numeric designations employed in the block diagrams and signal schematics to aid in identification. Following the component schematics are schematics of multiple-use elements, saturated flip-flop and chopper stabilized d-c operational amplifiers (figures 5-63 and 5-64).

1. Interrogator Encoder

The basic system repetition rate of 200 cps is generated by an astable multivibrator driving a bistable multivibrator (see figure 5-1).

The gate generated by the bistable multivibrator is used as a system sampling gate. Its duration is one-half of the period between cycles or 2.5 milliseconds.

The gate is also differentiated to form positive and negative spikes at leading and trailing edges, respectively.

The control coder employs a delay line with taps corresponding to desired time delay spacings between pulses 1 and 2 and pulses 2 and 3. Delay between pulse no. 1 and pulse no. 2 is 12 microseconds. A delayed pulse (pulse no. 2) is amplified and shaped and coupled to the mixer-amplifier. The delay between pulse no. 2 and pulse no. 3 is determined by the coarse altitude code wheel selecting a ground for a pickup amplifier on the control coder corresponding to the coarse altitude band in which the present or projected altitude is located. A delayed pulse (pulse no. 3) is amplified and shaped and coupled to the mixer-amplifier and the vernier coder.

The vernier coder uses a linear sweep generator to produce a pair of pulses delayed in time with respect to pulse no. 3, proportional to the altitude vernier d-c input voltage.

The gate generator is a simple flip-flop triggered on by pulse no. 3 and reset by pulse no. 5.

The sweep generator produces a linear sweep voltage proportional to time for the duration of the gate.

Isolation amplifiers decouple the sweep generator from the following circuits to prevent interaction which might cause sweep non-linearities. Clamping of sweeps to a d-c level permits vernier adjustments of delays to compensate for sweep generator delay irregularities and to provide a fixed time delay in addition to the continuously variable delay.

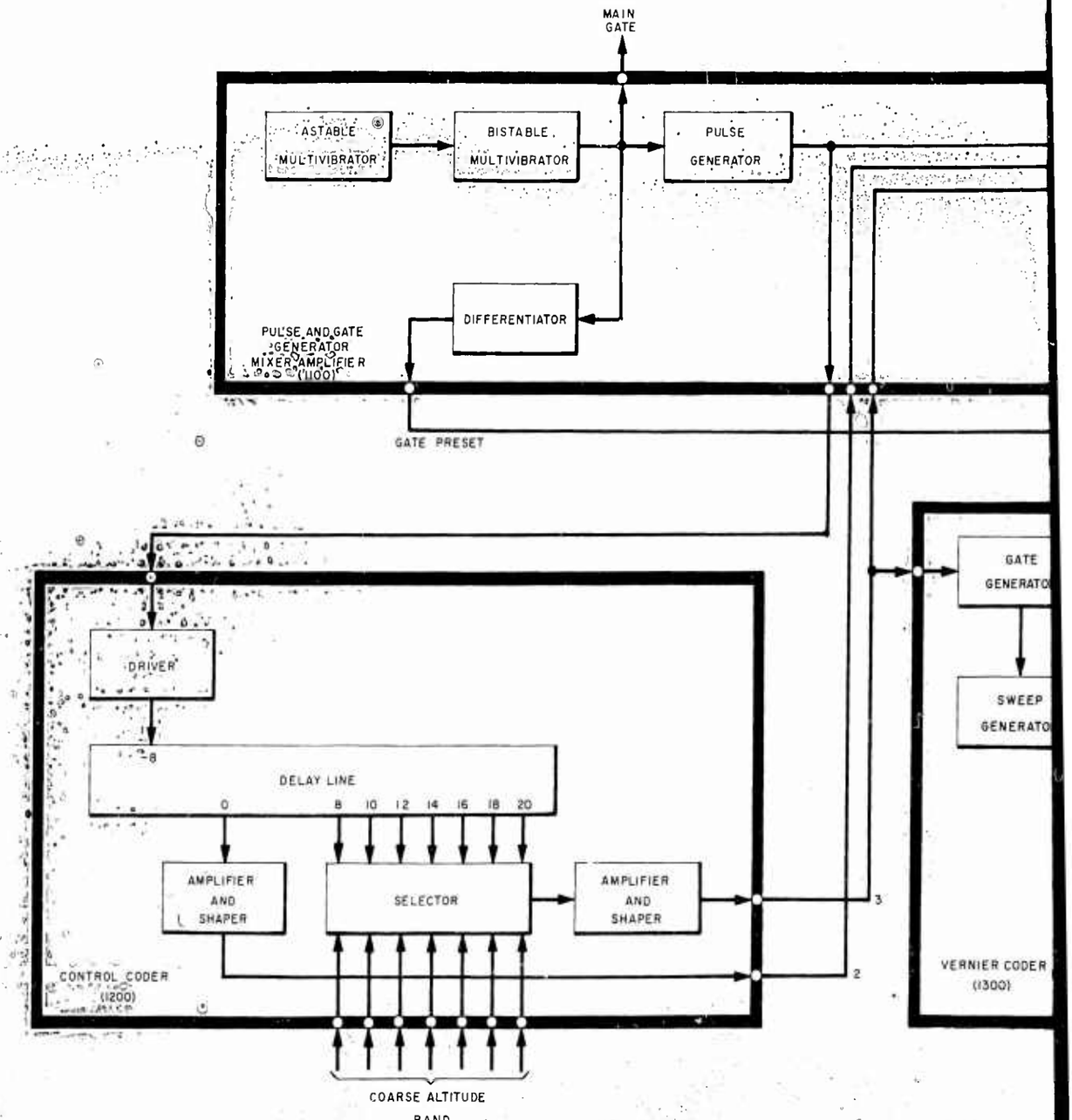
Comparators and pulse generators compare the sweep with the d-c reference voltage, generating pulses at the times the sweep voltages exceed the reference voltage.

The clamp voltage selector selects one of two clamp voltages to provide two positions for pulse no. 4 with respect to pulse no. 5. Both pulse no. 4 and pulse no. 5 are coupled to the mixer-amplifier.

The mixer-amplifier accepts all five input pulses and combines them in a five-pulse train. Isolation amplifiers decouple the amplifiers from the following circuits.

2. Interrogator Decoder

In the interrogator decoder block diagram, shown in figure 5-2 received video pulses are applied to the delay generator where they are delayed, amplified, and shaped into square pulses. Output signals correspond to delays of 4, 6, 8, 10, 12 and 20 microseconds.


MAIN GATE
ASTABLE MULTIVIBRATOR
BISTABLE MULTIVIBRATOR
PULSE GENERATOR
DIFFERENTIATOR
PULSE AND GATE GENERATOR MIXER AMPLIFIER (1100)
GATE PRESET
DRIVER
8
DELAY LINE
0
8
10
12
14
16
18
20
AMPLIFIER AND SHAPER
SELECTOR
AMPLIFIER AND SHAPER
3
2
CONTROL CODER (1200)
COARSE ALTITUDE BAND
GATE GENERATO
SWEEP GENERATO
VERNIER CODER (1300)

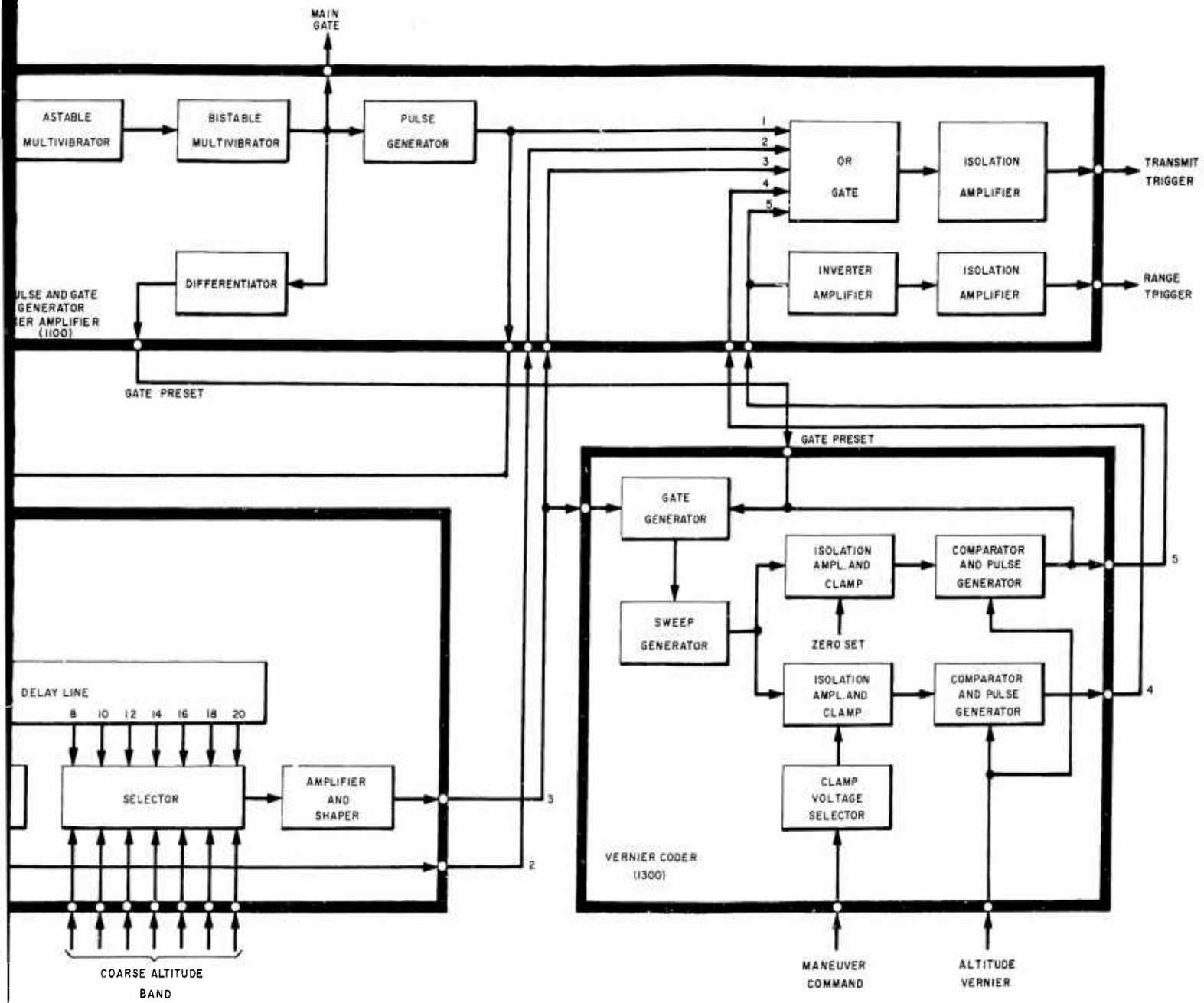
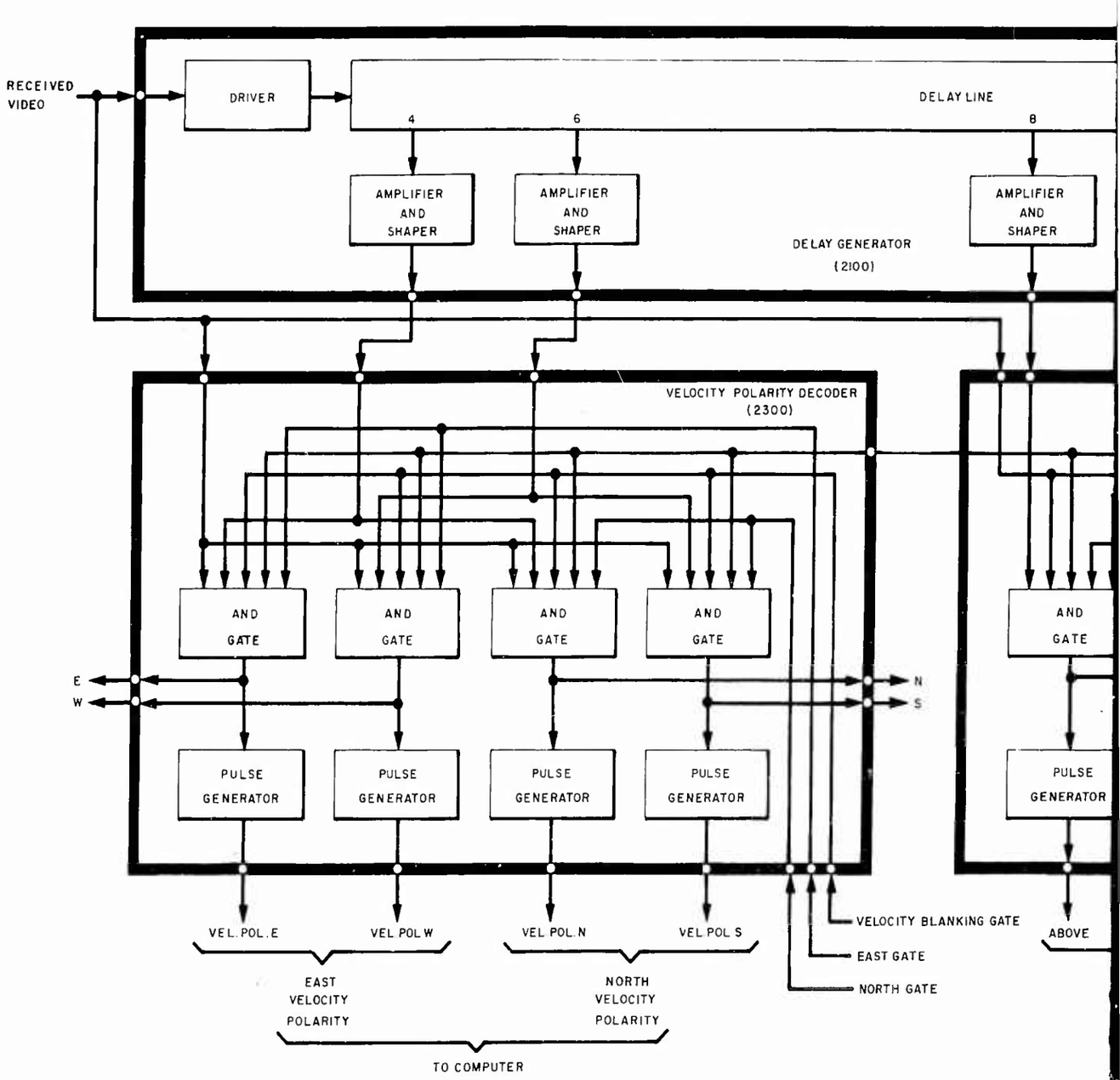


FIGURE 5-1
INTERROGATOR ENCODER (1000)


RECEIVED VIDEO
DRIVER
DELAY LINE
4
6
8
AMPLIFIER AND SHAPER
AMPLIFIER AND SHAPER
AMPLIFIER AND SHAPER
DELAY GENERATOR (2100)
VELOCITY POLARITY DECODER (2300)
AND GATE
AND GATE
AND GATE
AND GATE
AND GATE
E
W
N
S
PULSE GENERATOR
PULSE GENERATOR
PULSE GENERATOR
PULSE GENERATOR
PULSE GENERATOR
VEL. POL. E
VEL POL W
VEL POL. N
VEL POL S
VELOCITY BLANKING GATE
ABOVE
EAST GATE
NORTH GATE
EAST VELOCITY POLARITY
NORTH VELOCITY POLARITY
TO COMPUTER


1

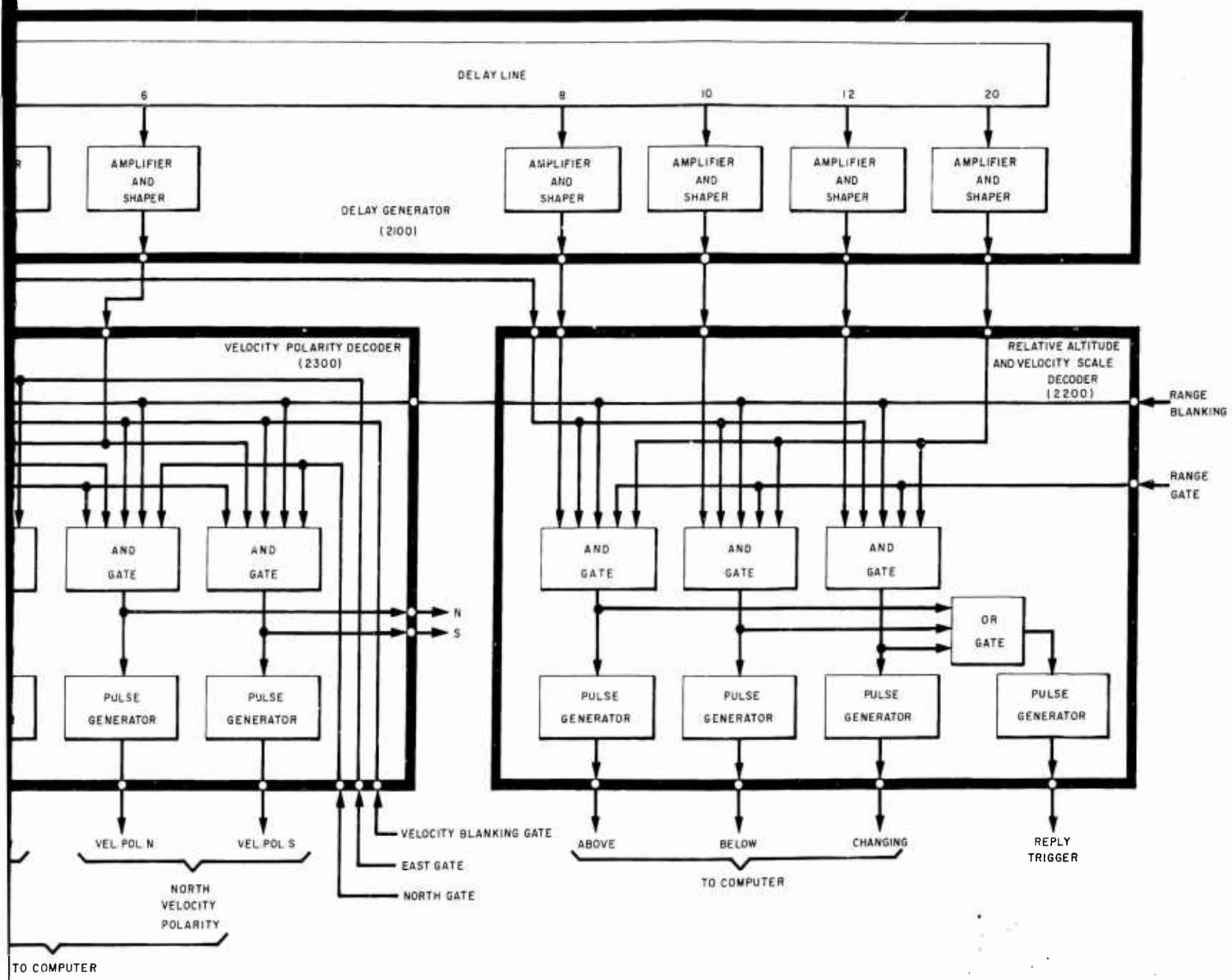
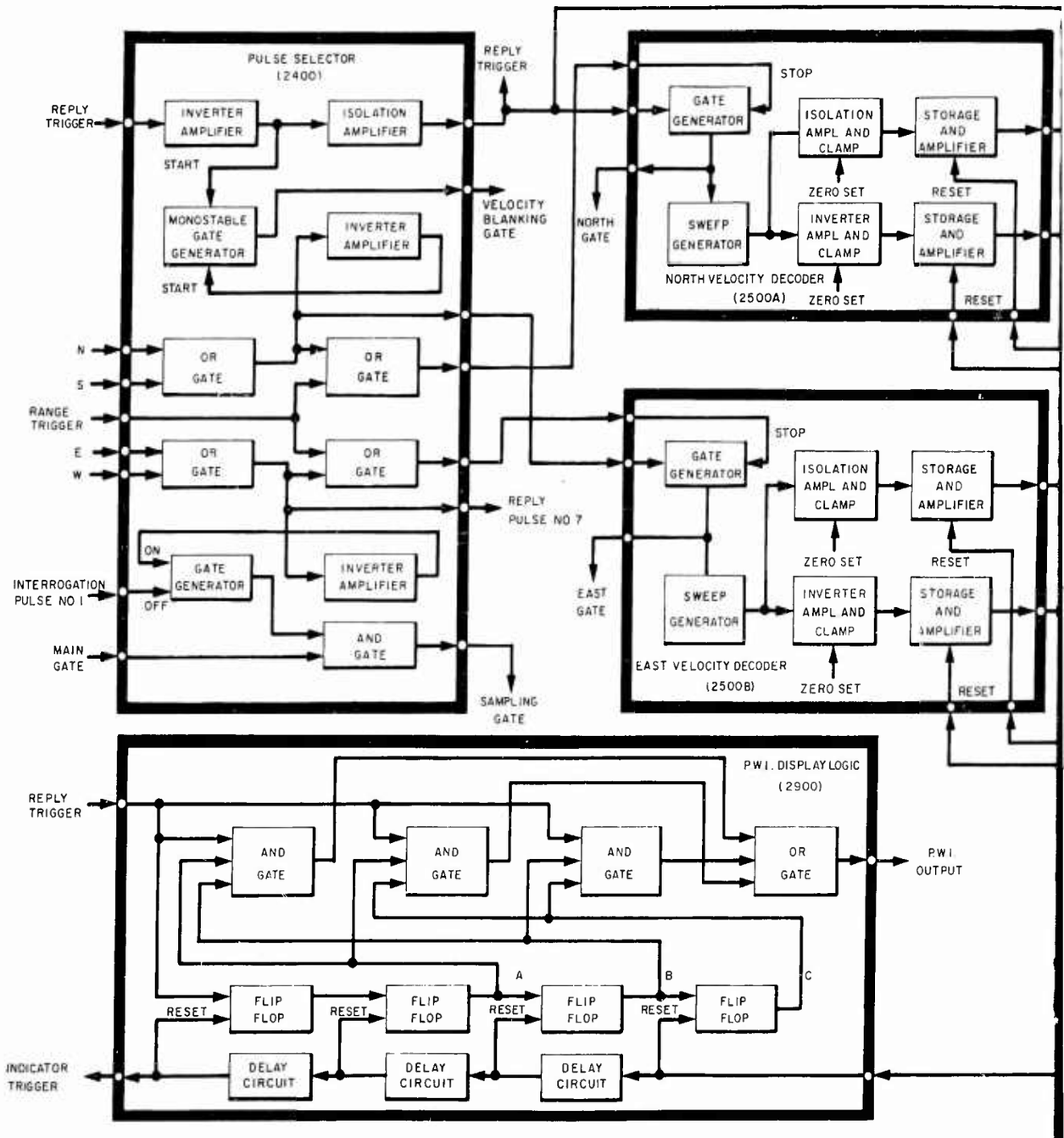


FIGURE 5-2

INTERROGATOR DECODER (2000) (SHEET 1 OF 2)


PULSE SELECTOR
(2400)
REPLY TRIGGER
INVERTER AMPLIFIER
ISOLATION AMPLIFIER
START
MONOSTABLE GATE GENERATOR
INVERTER AMPLIFIER
START
N
S
RANGE TRIGGER
E
W
OR GATE
OR GATE
OR GATE
OR GATE
ON
GATE GENERATOR
OFF
INVERTER AMPLIFIER
INTERROGATION PULSE NO 1
MAIN GATE
AND GATE
REPLY TRIGGER
VELOCITY BLANKING GATE
NORTH GATE
REPLY PULSE NO 7
EAST GATE
SAMPLING GATE
STOP
GATE GENERATOR
ISOLATION AMPL AND CLAMP
STORAGE AND AMPLIFIER
ZERO SET
RESET
SWEEP GENERATOR
INVERTER AMPL AND CLAMP
STORAGE AND AMPLIFIER
NORTH VELOCITY DECODER
(2500A)
ZERO SET
RESET
STOP
GATE GENERATOR
ISOLATION AMPL AND CLAMP
STORAGE AND AMPLIFIER
ZERO SET
RESET
SWEEP GENERATOR
INVERTER AMPL AND CLAMP
STORAGE AND AMPLIFIER
EAST VELOCITY DECODER
(2500B)
ZERO SET
RESET
P.W.I. DISPLAY LOGIC
(2900)
REPLY TRIGGER
AND GATE
AND GATE
AND GATE
OR GATE
P.W.I. OUTPUT
A
B
C
RESET
FLIP FLOP
RESET
FLIP FLOP
RESET
FLIP FLOP
RESET
FLIP FLOP
INDICATOR TRIGGER
DELAY CIRCUIT
DELAY CIRCUIT
DELAY CIRCUIT

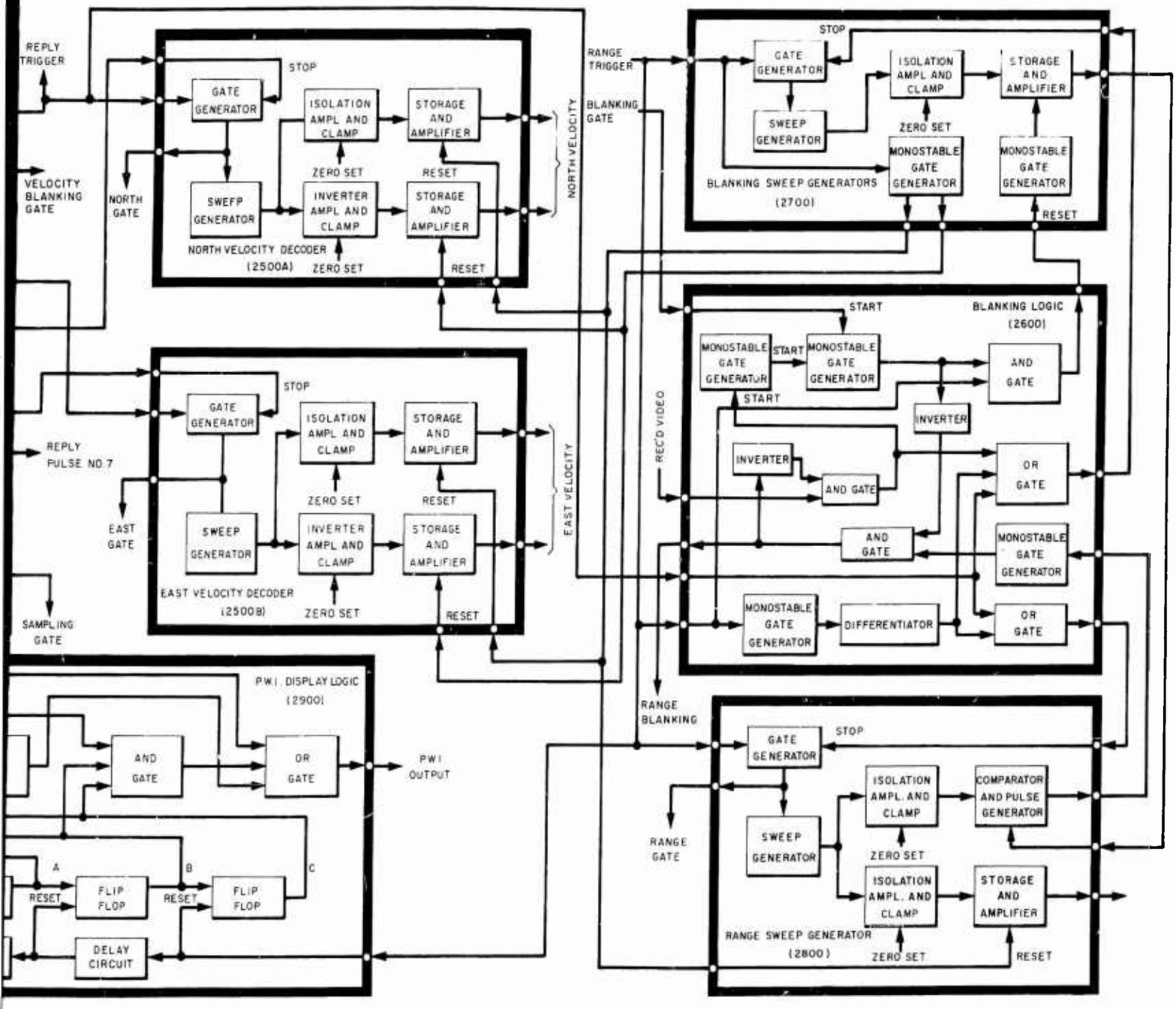


FIGURE 5-2.

INTERROGATOR DECODER (2000) (SHEET 2 OF 2)

The 8, 10, 12 and 20-microsecond delayed pulses are compared with the undelayed video pulses in the relative altitude decoder. If coincidence occurs in any of these three AND gates, a pulse appears at the corresponding output terminals. This reply trigger pulse is generated to start the velocity decoding, and complete the ranging measurements.

In the velocity polarity decoder the four- and six-microsecond delayed pulses are compared with the received video signal. In addition, gates are applied to separate the north and east polarity signals from each other, and to blank improper decoding of north or east components near or at zero magnitude. When video coincidence occurs between the four- or six-microsecond delayed signal and the undelayed video, an output pulse is generated provided that the appropriate north or east velocity gate is also present. The velocity polarity pulses are then coupled to the computer and to the north and east velocity decoders.

The north velocity decoder accepts a reply trigger pulse to start a linear velocity voltage sweep. The sweep is terminated when a north/south velocity polarity signal is received which resets the velocity gate generator. The sweep is also inverted, and both positive and negative sweep voltages are stored and peak detected to provide a bipolar north velocity voltage on two wires which is maintained until reset by the next range trigger pulse.

The east velocity decoder is identical to the north velocity decoder except that it is triggered on by the north/south velocity polarity signal and off by the east-west velocity polarity signal.

A sampling gate generator is also in the pulse selector. A flip-flop is triggered on by the east/west velocity polarity signal of a received pulse train; the off trigger is the next following interrogation pulse no. 1. Thus, when a correctly coded reply signal is received, a long gate is generated which is used to accept the main gate signal for use as a sampling gate in the computer. If no correctly coded reply signal is received no sampling gate is sent to the computer.

The range blanking signal is applied to the relative altitude decoder, velocity scale decoder, and the velocity polarity decoder.

The range measurement circuits consist of a range sweep generator, a blanking sweep generator, and a blanking logic circuit.

The range trigger pulse starts the voltage sweep of the range sweep generator. This sweep is stopped by a reset pulse from the blanking logic unit. The peak voltage reached by the sweep is stored in the voltage storage circuit and coupled to the computer as a range voltage. The voltage storage circuit is reset by the next following range trigger. A range gate is extracted from the gate generator to gate the relative altitude decoder and velocity scale decoder to accept only reply signals from transponders within a predetermined range.

The range trigger pulse also starts the blanking sweep generator voltage sweep which continues until reset by either the gated video (third pulse of a non-threatening transponder) or the coincidence trigger pulse. The peak voltage reached by this sweep is stored and applied to the comparator of the range sweep generator. By means of the zero set adjustments the blanking sweep generator voltage output is caused to produce a pulse output from the range sweep generator which precedes the coincidence trigger of the next cycle by a small time interval. This pulse is used for range blanking.

The blanking logic unit accepts the range trigger pulse and generates a monostable gate having a time duration equivalent to the range of the interrogator system. The gate is differentiated to produce a pulse at its trailing edge. This pulse is combined with the reply trigger pulse in an OR gate, such that the earlier of the two pulses resets the range sweep generator gate.

The gated video (third pulse of a non-threatening transponder) also starts a monostable gate generator which sets another monostable gate generator. The second gate generator output is coupled to an AND gate to inhibit the blanking sweep storage reset pulse. The duration of the sum of the two gates is slightly longer than one system cycle. A blanking gate from the computer, indicating that the earliest coincidence trigger is from a non-threatening aircraft and should be blanked also starts the second gate generator. Therefore, if a blanking gate is present or if the reply trigger is inhibited, then the range trigger is prevented from resetting the blanking sweep storage by means of an AND gate.

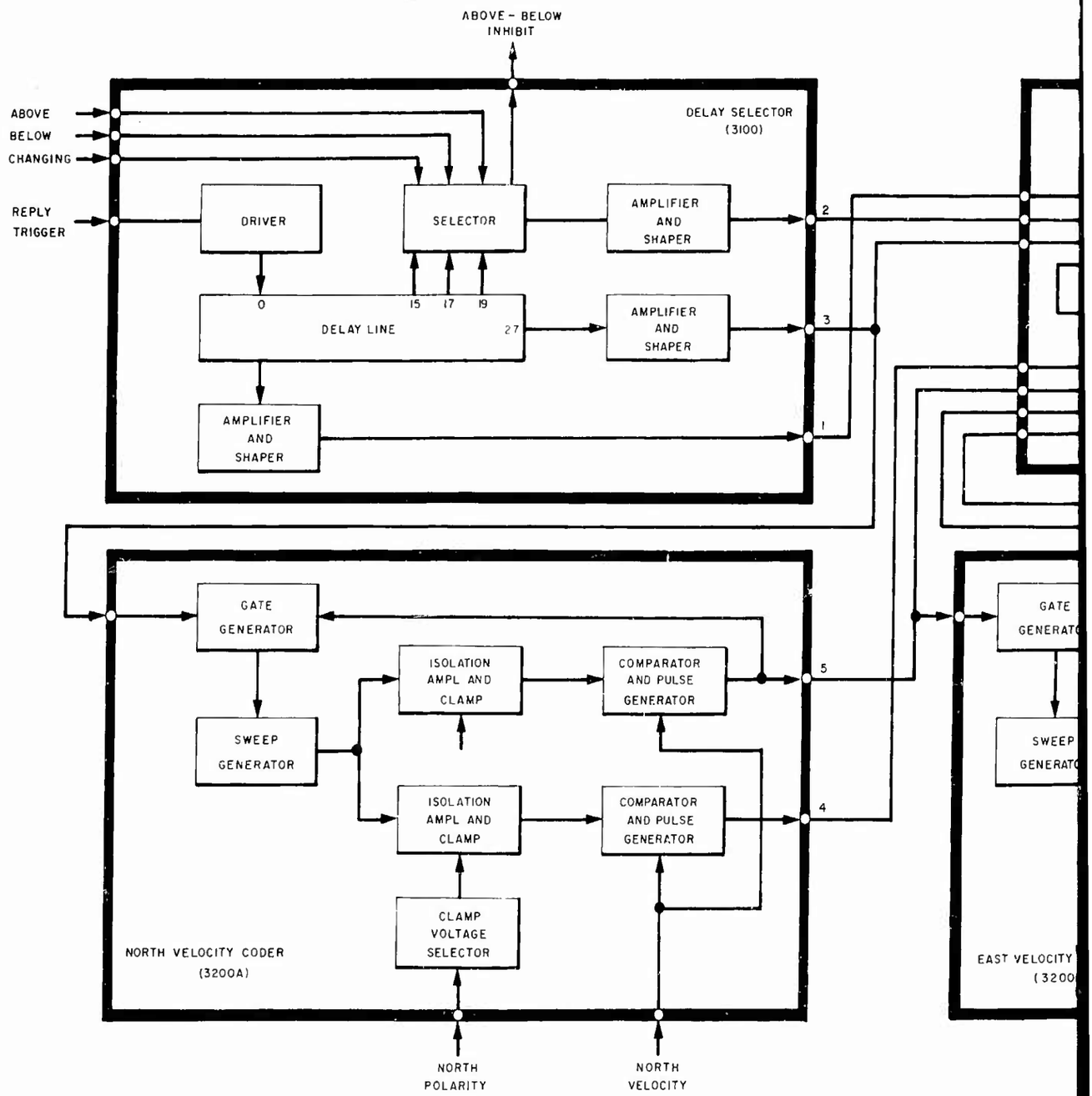
The storage reset inhibiting gate is also used to accept the range blanking pulse generated by the range sweep generator, passing through a monostable gate generator and thence to an AND gate. The resultant signal is the range blanking signal.

3. Transponder Encoder

The transponder encoder is driven by the reply trigger and modulates the transmit trigger and suppressor output signal with information concerning the vector velocity of the transponder aircraft. A block diagram of the transponder encoder is shown in figure 5-3.

The reply trigger is coupled into the delay selector of the transponder encoder where it drives a delay line. The following three pulses are tapped from this delay line:

- pulse no. 1 is chosen according to the velocity scale factor and is placed in a fixed time prior to pulse no. 3.
- pulse no. 2 is chosen according to the relative altitude of the interrogator input signal and is likewise placed in one of three positions. A climbing signal, if present, selects one position. If no climbing signal exists, an early trigger, if present, selects a second position. If neither a climbing signal nor any early trigger signal is present the third position is chosen.


ABOVE - BELOW
INHIBIT
ABOVE
BELOW
CHANGING
REPLY
TRIGGER
DELAY SELECTOR
(3100)
DRIVER
SELECTOR
AMPLIFIER
AND
SHAPER
2
0
15
17
19
DELAY LINE
27
AMPLIFIER
AND
SHAPER
3
AMPLIFIER
AND
SHAPER
1
GATE
GENERATOR
ISOLATION
AMPL AND
CLAMP
COMPARATOR
AND PULSE
GENERATOR
5
SWEEP
GENERATOR
ISOLATION
AMPL AND
CLAMP
COMPARATOR
AND PULSE
GENERATOR
4
CLAMP
VOLTAGE
SELECTOR
NORTH VELOCITY CODER
(3200A)
NORTH
POLARITY
NORTH
VELOCITY
GATE
GENERAT
SWEEP
GENERAT
EAST VELOCITY
(3200

1

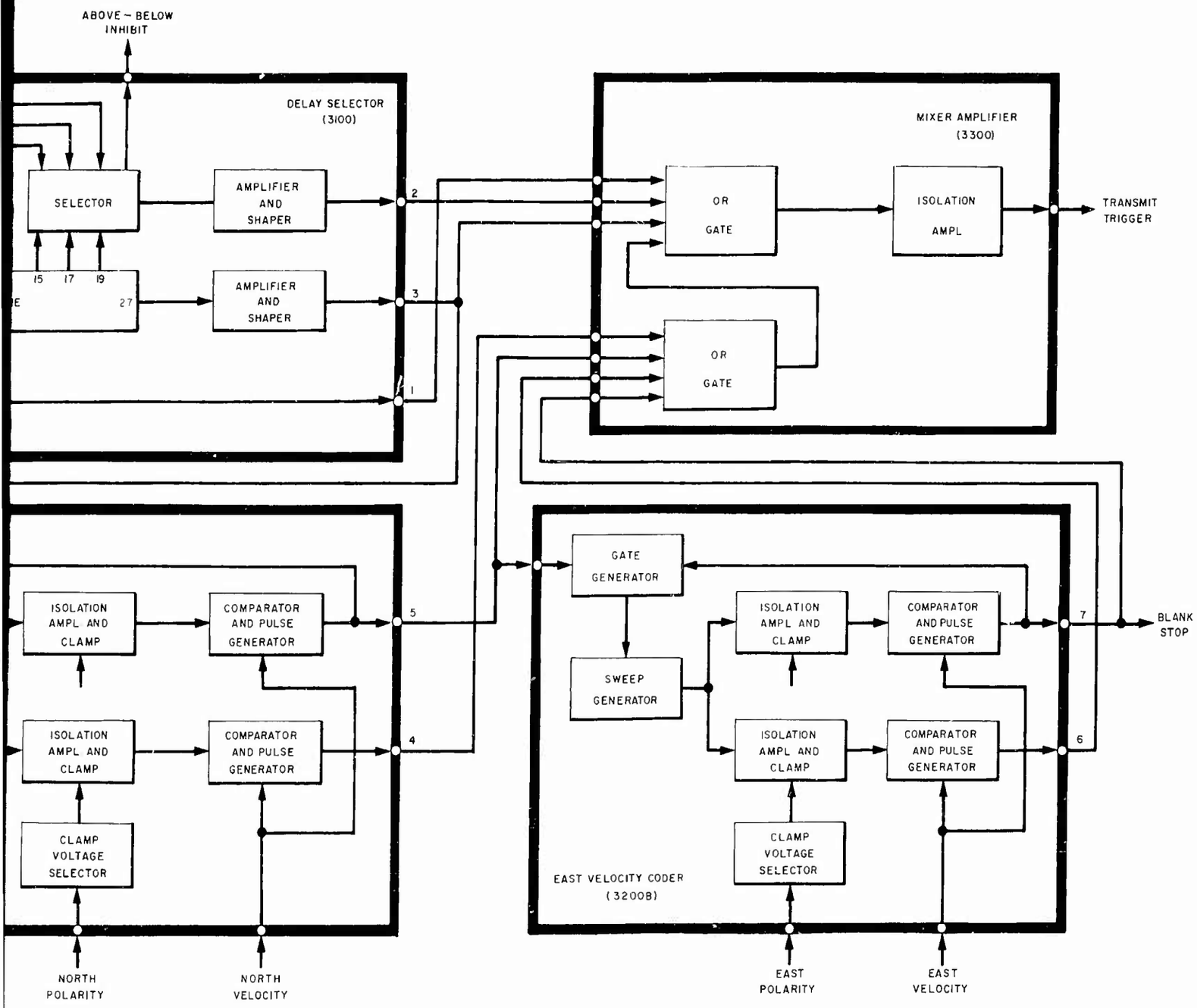


FIGURE 5-3

TRANSPONDER ENCODER (3000)

- pulse no. 3 is delayed by a fixed time from the reply trigger pulse and is coupled to the north velocity coder where it triggers a flip-flop gate generator which activates a linear sweep generator.

The voltage sweep of the linear sweep generator is coupled to two isolation amplifiers which prevent interaction of the pulse generating circuits with the sweep.

Pulse no. 5 is generated from a comparison between the linear sweep and a voltage proportional to the north velocity component of the aircraft. This pulse is initiated when the sawtooth sweep voltage exceeds the north velocity voltage and thus the delay of pulse no. 5 is proportional to the north velocity of the aircraft.

Pulse no. 4 is generated in a manner similar to pulse no. 5 except that the sweep signal is clamped to a different voltage level in accordance with the north polarity input. One of two clamp voltages is selected. Clamping of the sweep to a preset level provides an artificial sweep starting time and therefore a different delay period for any given velocity reference voltage. The clamp voltage selector can be set such that pulse no. 4 precedes pulse no. 5 by either four or six microseconds.

Pulse no. 5 is coupled to the flip-flop gate generator to reset the circuit and thus terminate the gate and sweep voltage. It is also coupled to the east velocity coder which acts in the same manner as the north velocity coder just described. Pulses no. 6 and 7 are generated in this unit in the same way that pulses 4 and 5 were generated in the north velocity coder.

Pulses 1 through 7 are coupled to the mixer-amplifier and combined into a single signal consisting of all seven pulses in time sequence. An isolation amplifier is used to provide a low impedance driving source of the 7-inch train.

Pulse no. 5 is generated from a comparison between the linear sweep and a voltage proportional to the north velocity component of the aircraft. This pulse is initiated when the sawtooth sweep voltage exceeds the north velocity voltage and thus the delay of pulse no. 5 is proportional to the north velocity of the aircraft.

Pulse no. 4 is generated in a manner similar to pulse no. 5 except that the sweep signal is clamped to a different voltage level in accordance with the north polarity input. One of two clamp voltages is selected. Clamping of the sweep to a preset level provides an artificial sweep starting time and therefore a different delay period for any given velocity reference voltage. The clamp voltage selector can be set such that pulse no. 4 precedes pulse no. 5 by either four or six microseconds.

Pulse no. 5 is coupled to the flip-flop gate generator to reset the circuit and thus terminate the gate and sweep voltage. It is also coupled to the east velocity coder which acts in the same manner as the north velocity coder just

described. Pulses 6 and 7 are generated in this unit in the same way that pulses 4 and 5 were generated in the north velocity coder.

Pulses 1 through 7 are coupled to the mixer-amplifier and combined into a single signal consisting of all seven pulses in time sequence. The 7-pulse train is shaped for use as a suppressor output signal.

The 7-pulse train is also delayed by a 0.8-microsecond delay line to provide the specified pretriggering time for the suppressor signal. This output is the transmit trigger.

4. Transponder Decoder

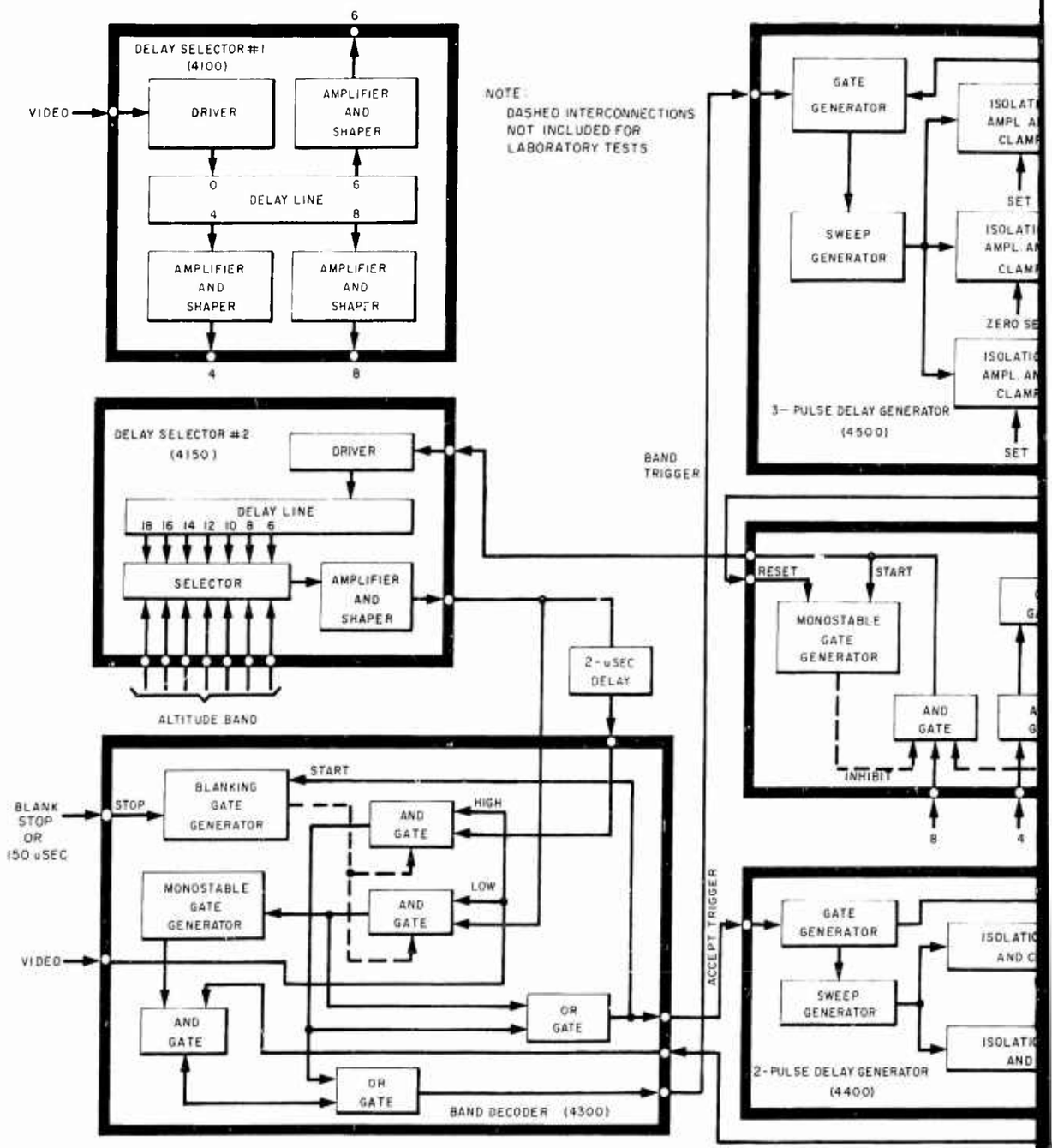
As shown in the block diagram, figure 5-4, the video pulse train is applied to the delay selector no. 1 where the entire signal is delayed by fixed times of 4, 6, and 8 microseconds. Separate outputs are provided for each delay time.

All three of these outputs are applied to the command decoder. Input no. 8 is compared with the undelayed video signal and if coincidence occurs between the undelayed video and the 8-microsecond delayed signal an output pulse is generated.

This coincidence output (coincident with interrogation pulse no. 2) is routed to the delay selector no. 2 where it is delayed an amount corresponding to the coarse altitude band of the transponder aircraft, as selected by the coarse altitude code wheel of the transponder aircraft. The delayed pulse is amplified, shaped, and coupled to the band decoder.

The band decoder unit compares the delayed output signal with the video pulses to determine if the video signal corresponds to either the selected altitude band or the band above. Comparison for the selected altitude band is performed in an AND gate which produces a low band output trigger pulse. For the band above the selected band, the delayed input signal is delayed an additional two microseconds and compared with video in another AND gate to produce a high band output trigger pulse. Both low band and high band output triggers are applied to an OR gate to produce the accept trigger signal. Both of these AND gates are blanked by a signal from the blanking gate generator.

The output trigger from the low band AND gate also triggers a 30-microsecond monostable multivibrator. A pulse delayed by 20 microseconds (from the two-pulse delay generator) is compared with this gate in an AND gate. The output of this AND gate is coupled to an OR gate in addition to the high band output trigger, to generate a band trigger pulse for triggering the three-pulse delay generator. With this technique the trigger for the three-pulse delay generator occurs at the time of the third input video pulse if the input code corresponds to the higher altitude band, and at 20 microseconds later than the third input video pulse if the input code corresponds to the same altitude band as that selected by the sensor.


DELAY SELECTOR #1
(4100)
VIDEO
DRIVER
AMPLIFIER AND SHAPER
DELAY LINE
AMPLIFIER AND SHAPER
AMPLIFIER AND SHAPER
NOTE
DASHED INTERCONNECTIONS NOT INCLUDED FOR LABORATORY TESTS
GATE GENERATOR
SWEEP GENERATOR
3— PULSE DELAY GENERATOR
(4500)
SET
ZERO SE
SET
DELAY SELECTOR #2
(4150)
DRIVER
DELAY LINE
18 16 14 12 10 8 6
SELECTOR
AMPLIFIER AND SHAPER
ALTITUDE BAND
BAND TRIGGER
2-uSEC DELAY
RESET
START
MONOSTABLE GATE GENERATOR
AND GATE
INHIBIT
BLANK STOP OR 150 uSEC
STOP
BLANKING GATE GENERATOR
START
AND GATE
HIGH
MONOSTABLE GATE GENERATOR
AND GATE
LOW
VIDEO
AND GATE
OR GATE
OR GATE
BAND DECODER (4300)
ACCEPT TRIGGER
GATE GENERATOR
SWEEP GENERATOR
2-PULSE DELAY GENERATOR
(4400)

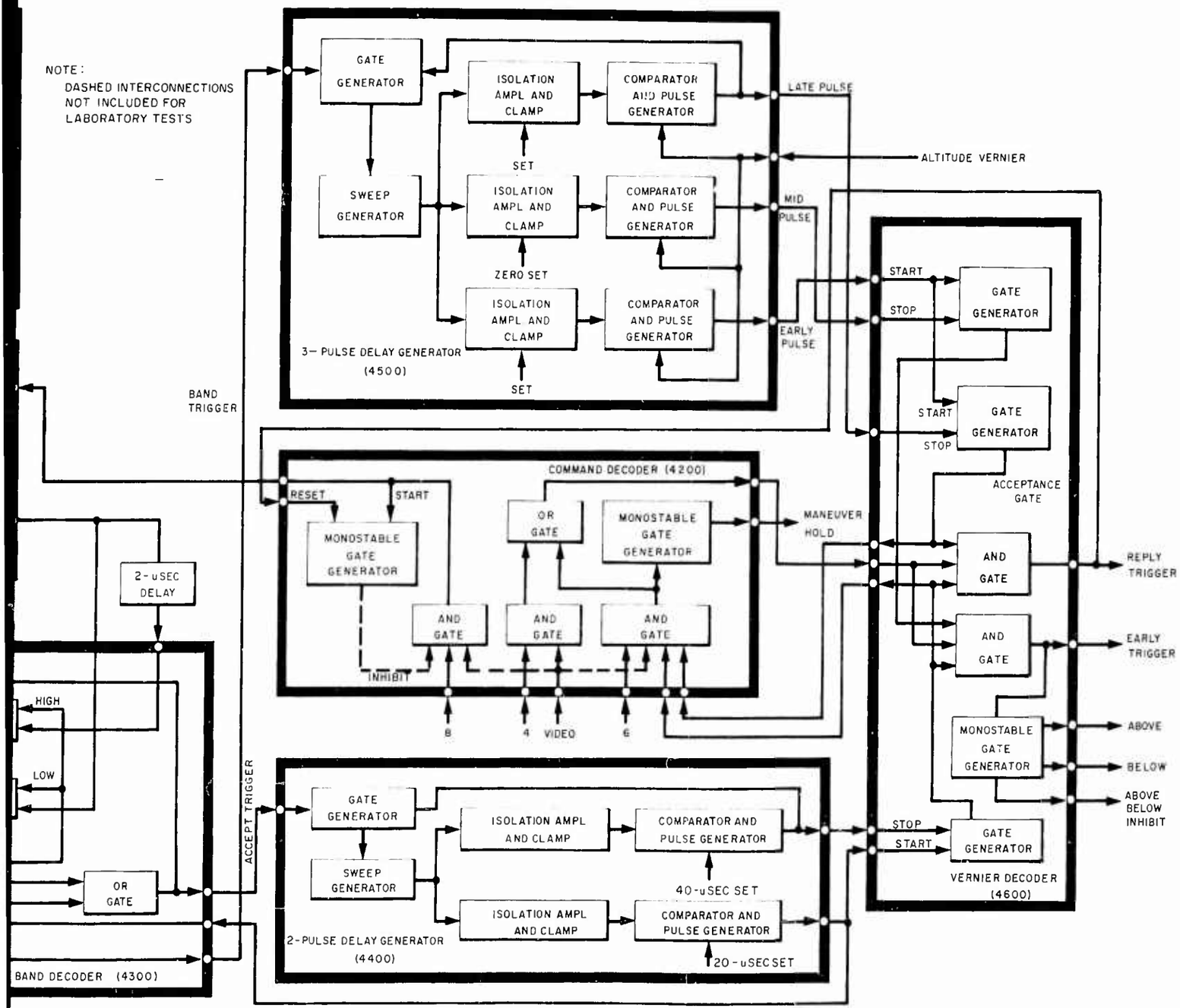


FIGURE 5 4

TRANSPONDER DECODER (4000)

The two-pulse delay generator is triggered by the accept trigger from the band decoder. This unit generates two pulses delayed 20 microseconds and 40 microseconds from the accept trigger. The generator is reset by the 40-microsecond delayed pulse.

The three-pulse delay generator is triggered by the band trigger pulse and generates three delayed pulses by means of a linear sweep generator. The altitude vernier control voltage from the altitude sensor is coupled to the three comparator circuits and controls the time delay of the three pulses. Delay of the middle pulse is proportional to the altitude vernier voltage. Delay of the early and late pulses is controlled by the clamp voltages set to obtain the required guard band.

The vernier decoder contains gating circuits for accepting or rejecting the altitude vernier pulse signal. An early gate is initiated by the early pulse and terminated by the middle pulse. An acceptance gate is also started by the early pulse, but terminated by the late pulse. These gates are coupled to two AND gates which are also gated by a 20-microsecond video gate. The video gate is positioned to accept only signals which occur within the altitude vernier code time interval. The vernier trigger pulse is also applied to the two AND gates. If coincidence with the acceptance gate occurs, a reply trigger is generated, and if coincidence with the early gate occurs an early trigger is generated. If an early trigger is generated, a monostable gate generator is set, indicating an above state to the transponder encoder. An absence of early trigger denotes below similarly.

The acceptance and video gates are also applied to an AND gate in the command decoder to determine if a maneuver command exists. Coincidence of the fifth interrogation pulse with a fourth pulse delayed six microseconds by the delay selector no. 1 in the presence of the acceptance and video gates sets the maneuver command monostable gate generator.

5. Interrogator Computer

The interrogator computer evaluates collision threats based on decoded and locally derived data and, if a risk exists, provides the intelligence to activate the appropriate maneuver display. A signal schematic of the computer is shown in figure 5-5.

The airspeed of the interrogating aircraft is resolved with respect to relative antenna bearing in the relative bearing servo. Inputs to the relative bearing motor amplifier, in addition to the bearing error signal, include:

- a heading error signal from the local transponder heading servo which cancels high frequency components of aircraft motion, resulting in data referenced to the average heading of the aircraft
- a fixed bias to compensate for the steady state velocity lag in the servo due to the 30-rpm antenna scan speed.

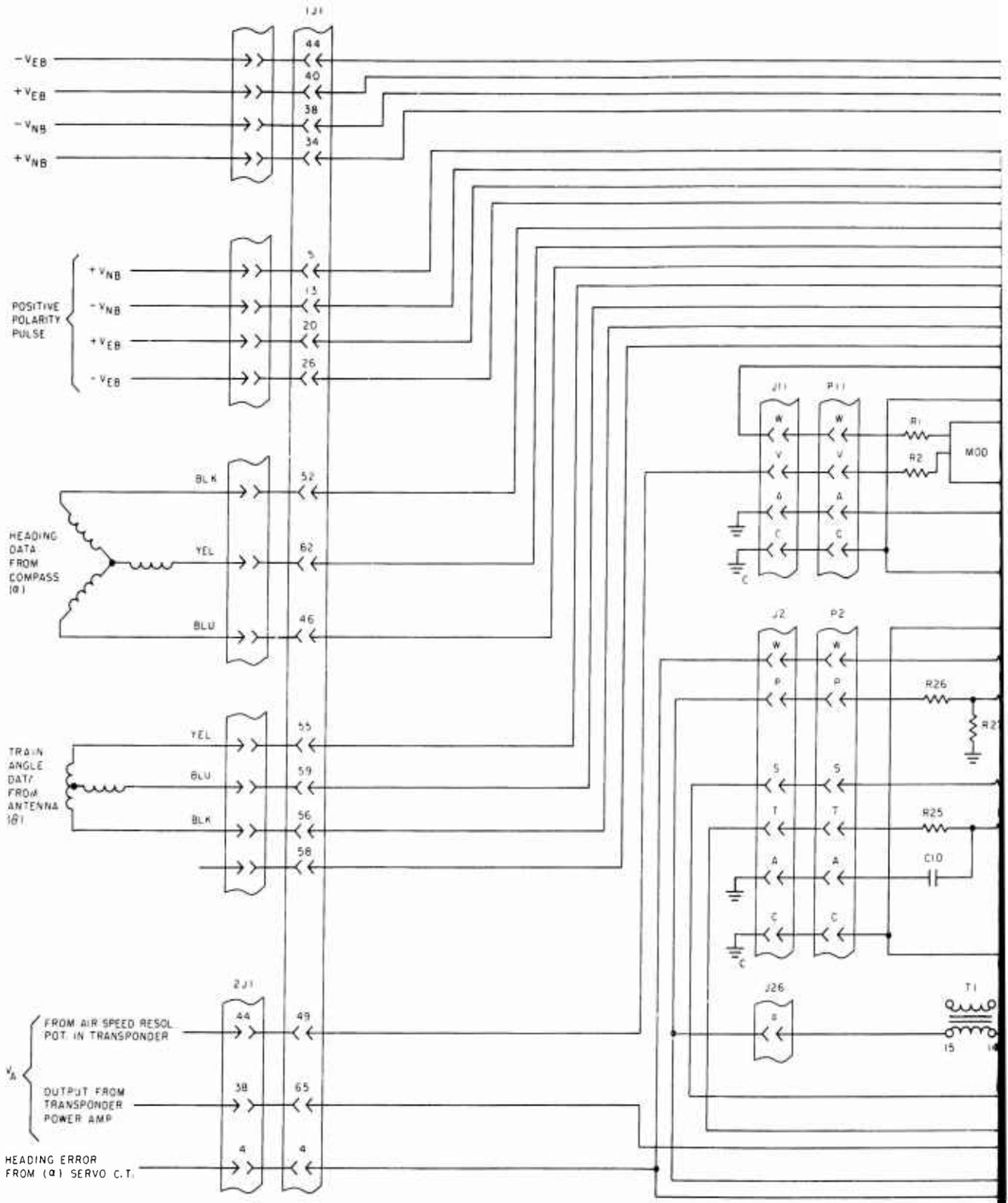
The decoded components of the transponding aircraft's airspeed are resolved with respect to antenna magnetic bearing in the magnetic bearing servo. The polarity of the airspeed components applied to the resolver is selected in the polarity control amplifier based on decoded reply data. The heading error signal from the local transponder is applied to this motor amplifier in reversed sense to recover the high frequency components, resulting in instantaneous data with respect to the external reference (magnetic north). The fixed bias is also applied as an input here to compensate for steady state velocity lag.

The resolver outputs constitute components of both aircraft's velocities normal to and parallel to the antenna bearing. The normal and radial components are summed with proper polarities in the normal velocity and radial velocity adders, respectively, to yield the corresponding components of the relative velocity between aircraft. Normal velocity signals are scaled so that the adder limits velocity samples to about 133 knots. This limit will not effect valid data in a collision or near collision case, but will minimize the effect of a single large error in the subsequent averaging process.

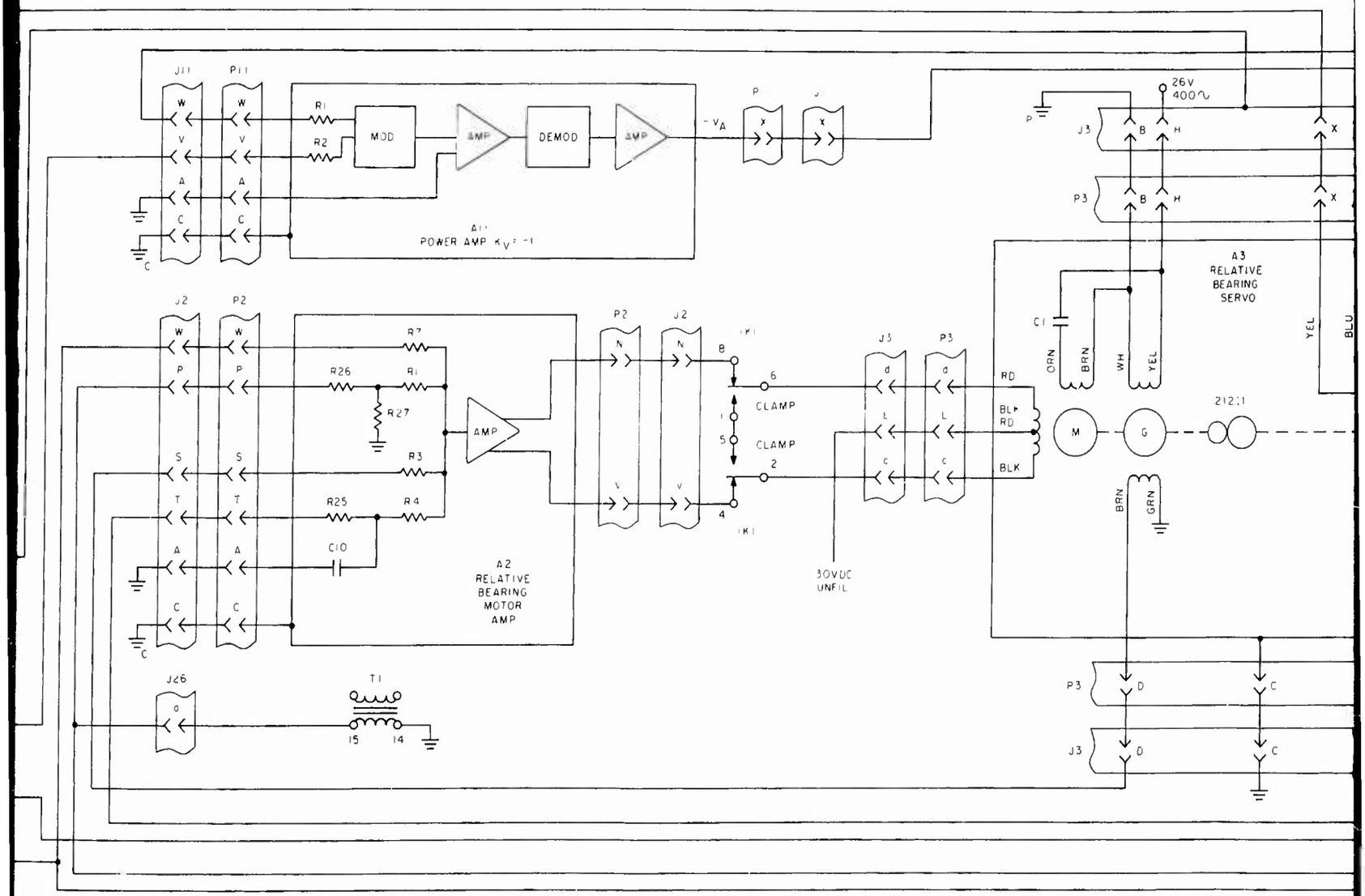
The radial component of relative velocity is scaled by a voltage divider in the range criterion comparator to analogs of the ranges which would be covered in 27 and 40 seconds. These range analogs are compared with the analog of actual range to determine the increment in which time-to-go lies. Actual range is also compared with a fixed 1/3 nautical mile bias to determine whether the minimum range limit has been violated. The results of these comparisons are the decisions on time-to-go and minimum range used in the Maneuver Logic.

Successive samples of the normal velocity and the velocity threshold (45 knots) analogs are summed in the normal velocity and velocity threshold integrators, respectively. The samples are gated in by the sample gate controller each time a complete reply is received, as indicated by the sample gate signal. The sums are read out and the integrators reset on leaving a given target, as indicated by the occurrence of two consecutive misses or a range change of more than 0.36 nautical miles. The derivation of the reset control signals is described below.

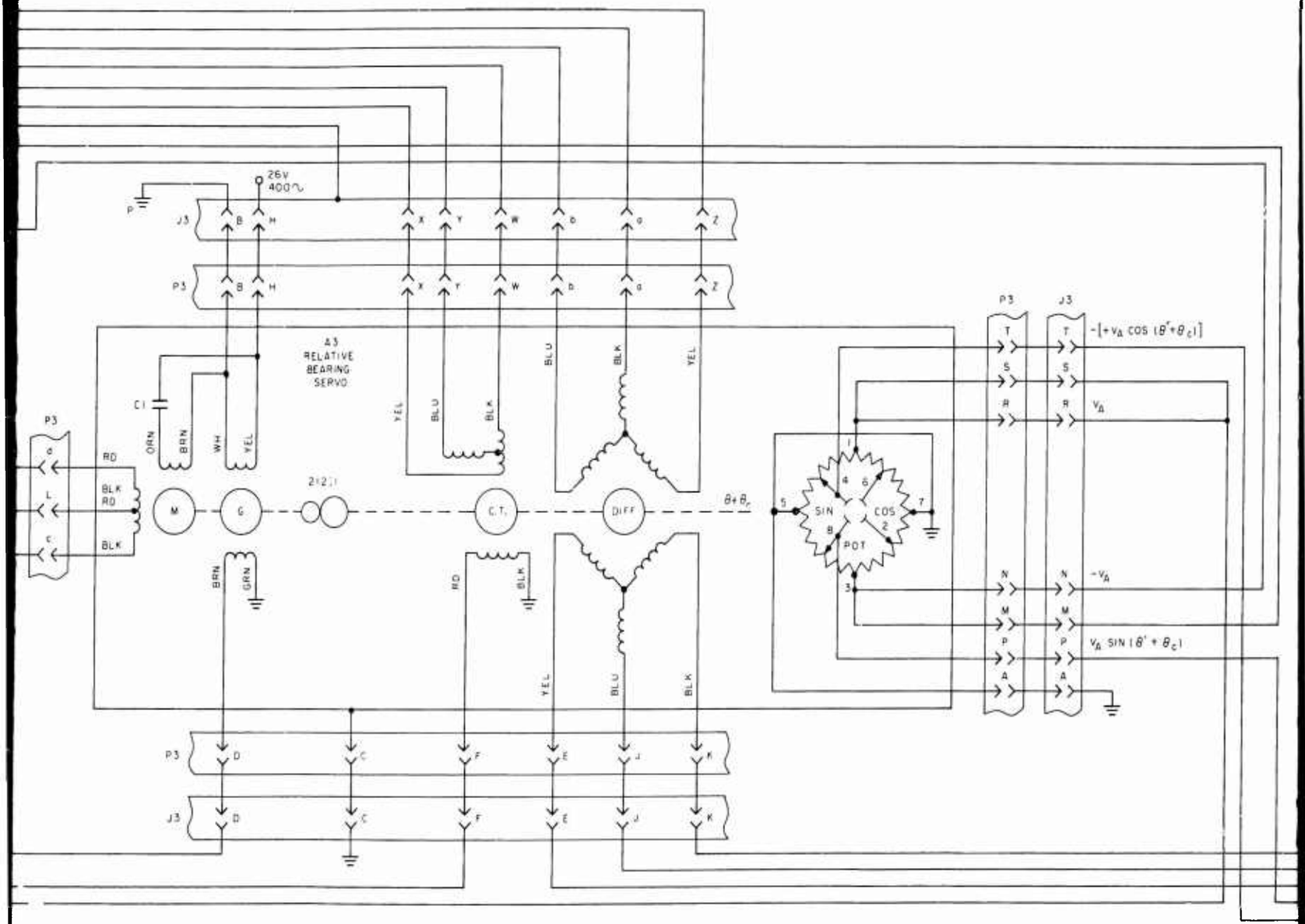
The sums of the normal velocity samples and the velocity threshold samples are compared in the normal velocity criterion comparator to evaluate the collision threat. This comparison is equivalent to comparing the normal velocity sample closest to the beam center with the velocity threshold, and this effectively locates the antenna beam centerline. It also has the added advantage of averaging out errors in the received velocity data. The result of this comparison is a decision on whether or not a collision threat exists, used in the Maneuver Logic. The output of the velocity threshold integrator is also compared with a fixed bias corresponding to more than two samples (about 100 knots). The result of this comparison is used to inhibit collision decision outputs based on one or two samples only.


J21
-VEB
+VEB
-VNB
+VNB
44
40
38
34
POSITIVE POLARITY PULSE
+VNB
-VNB
+VEB
-VEB
5
13
20
26
HEADING DATA FROM COMPASS (α)
BLK
YEL
BLU
52
62
46
TRAIN ANGLE DATA FROM ANTENNA (β)
YEL
BLU
BLK
55
59
56
58
J11
P11
W
V
A
C
R1
R2
MOD
J2
P2
P
S
T
R26
R25
C10
J26
T1
15
2J1
FROM AIR SPEED RESOL POT. IN TRANSPONDER
OUTPUT FROM TRANSPONDER POWER AMP
VA
HEADING ERROR FROM (α) SERVO C.T.
44
38
4
49
65
4

1

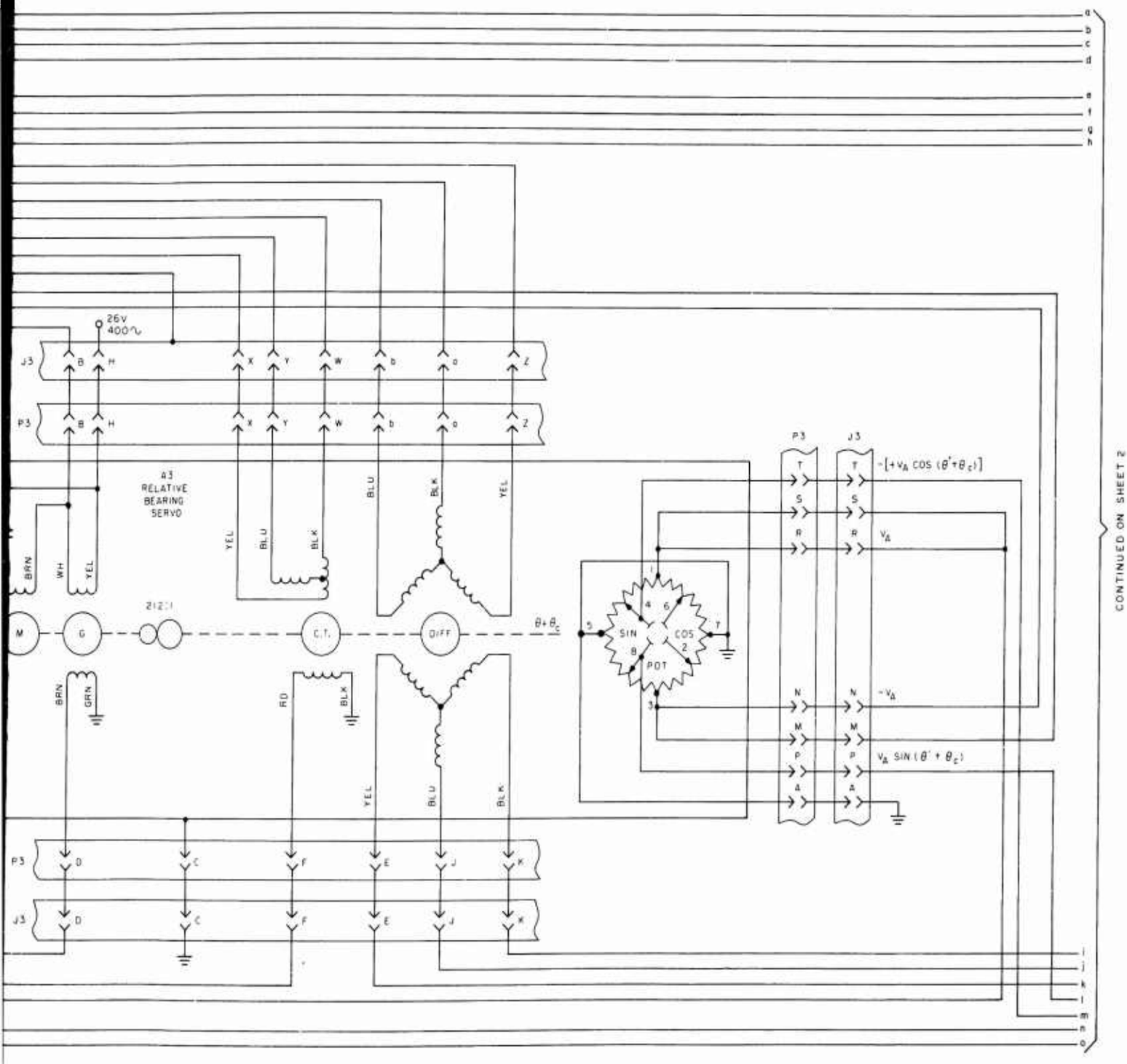

J11
P11
W
V
A
C
R1
R2
MOD
AMP
DEMOD
AMP
-VA
P
J
X
A1
POWER AMP
26V
400~
J3
P3
B
H
X
A3
RELATIVE
BEARING
SERVO
C1
ORN
BRN
WH
YEL
YEL
BLU
J2
P2
W
P
S
T
A
C
R7
R26
R1
R27
R3
R25
R4
C10
AMP
A2
RELATIVE
BEARING
MOTOR
AMP
N
V
B
6
CLAMP
5
CLAMP
2
4
K1
30VDC
UNFIL
d
L
c
RD
BLK
RD
BLK
M
G
2121
BRN
GRN
D
C
J26
T1
15
14

2



3

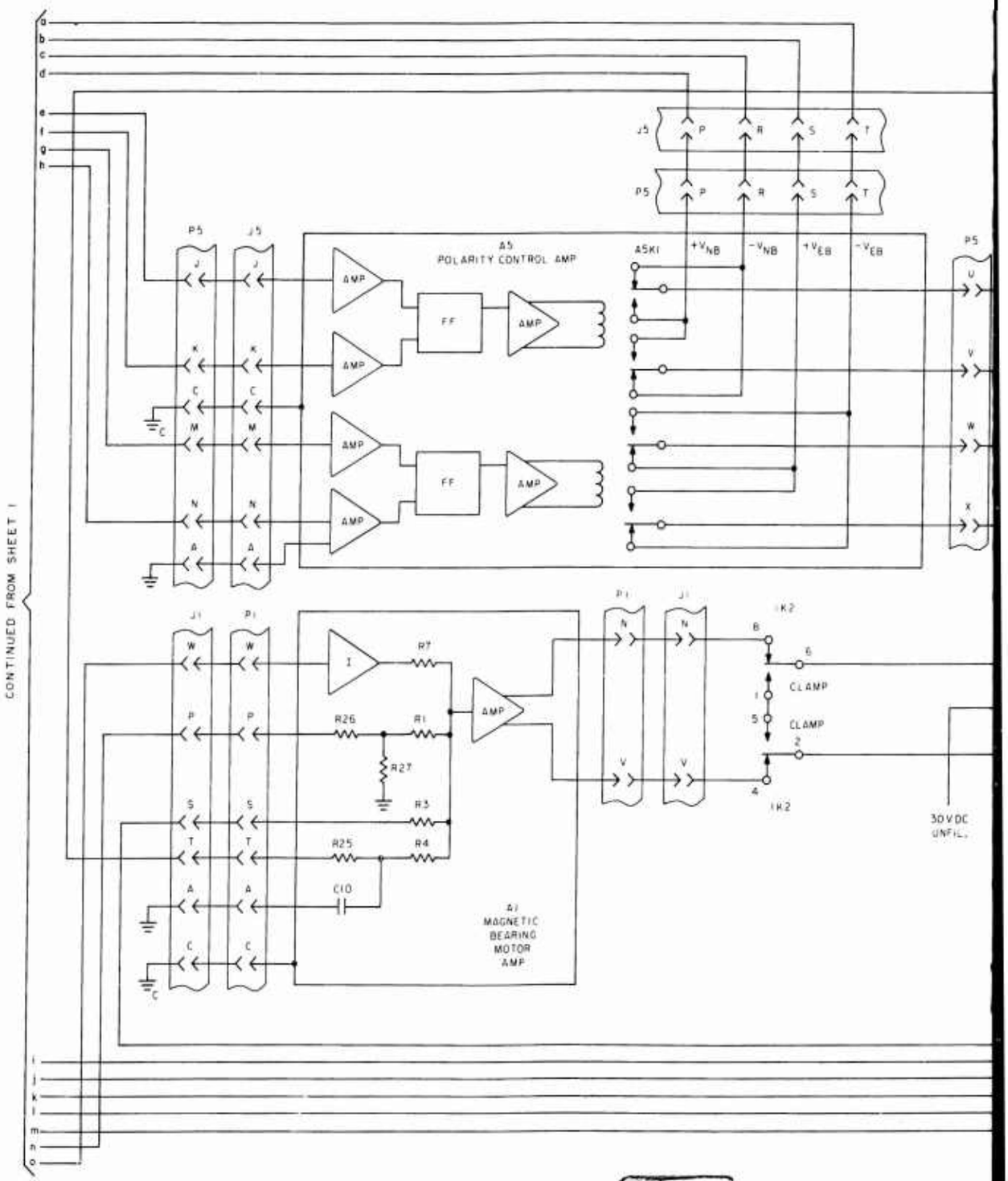
FIGURE 5-5
INTERROGATOR COMPUTER SIGNAL SC
(SHEET 1 OF 4)



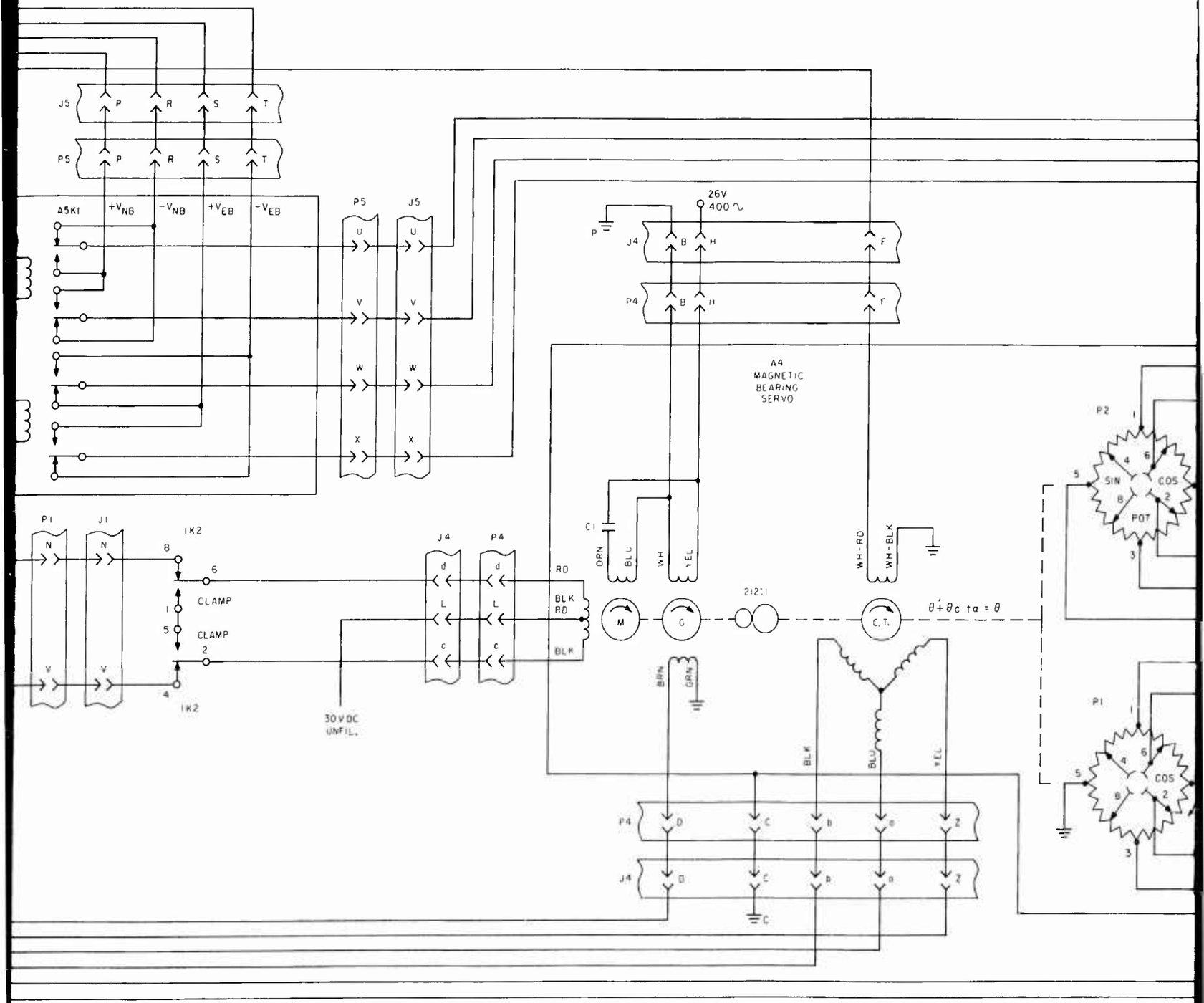
4

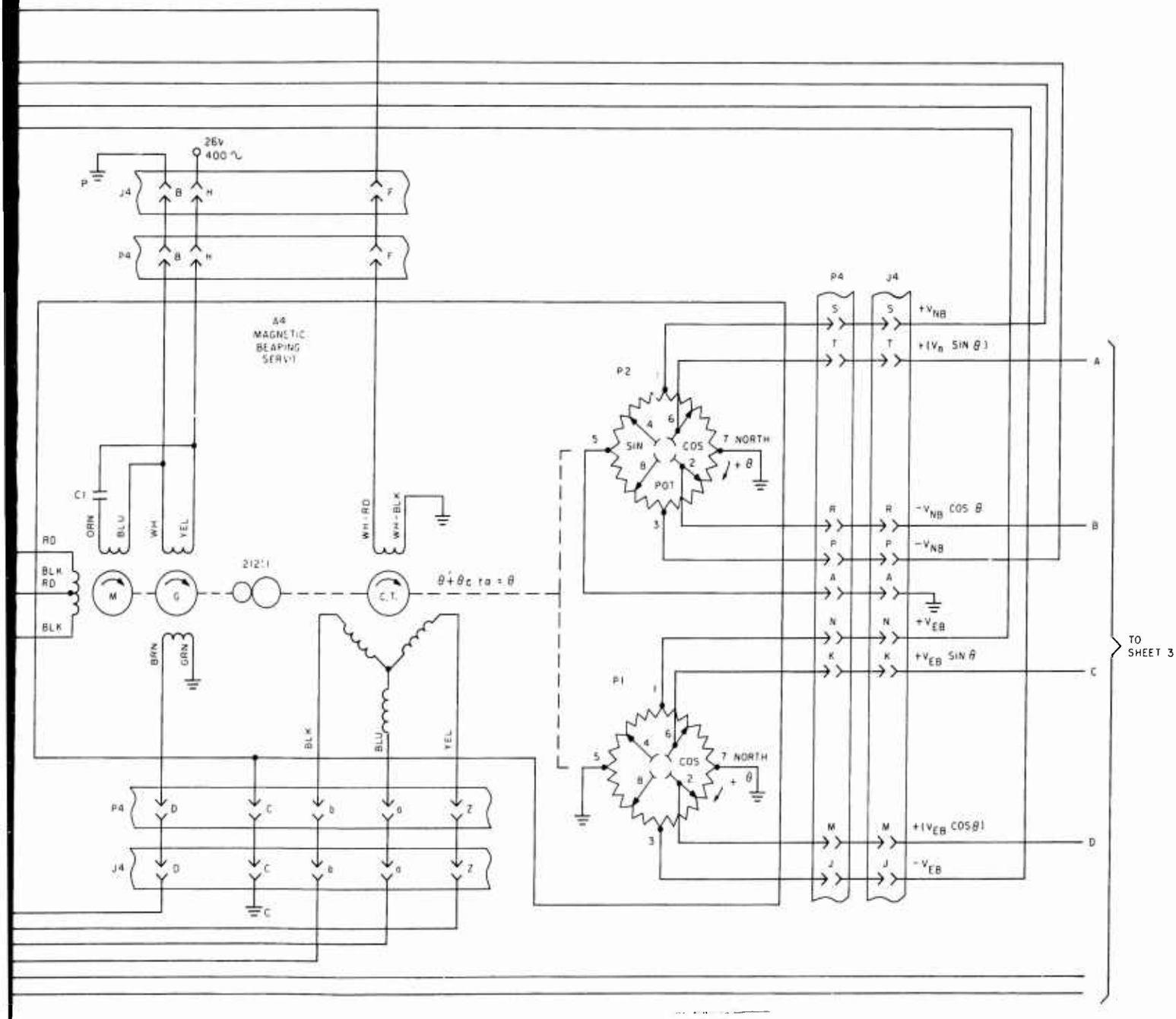
FIGURE 5-5

INTERROGATOR COMPUTER SIGNAL SCHEMATIC
(SHEET 1 OF 4)


CONTINUED FROM SHEET 1
A5
POLARITY CONTROL AMP
AMP
FF
ASKI
+V NB
-V NB
+V EB
-V EB
A1
MAGNETIC
BEARING
MOTOR
AMP
R7
R26
R1
R27
R3
R25
R4
C10
CLAMP
CLAMP
30 VDC
UNFIL.

1

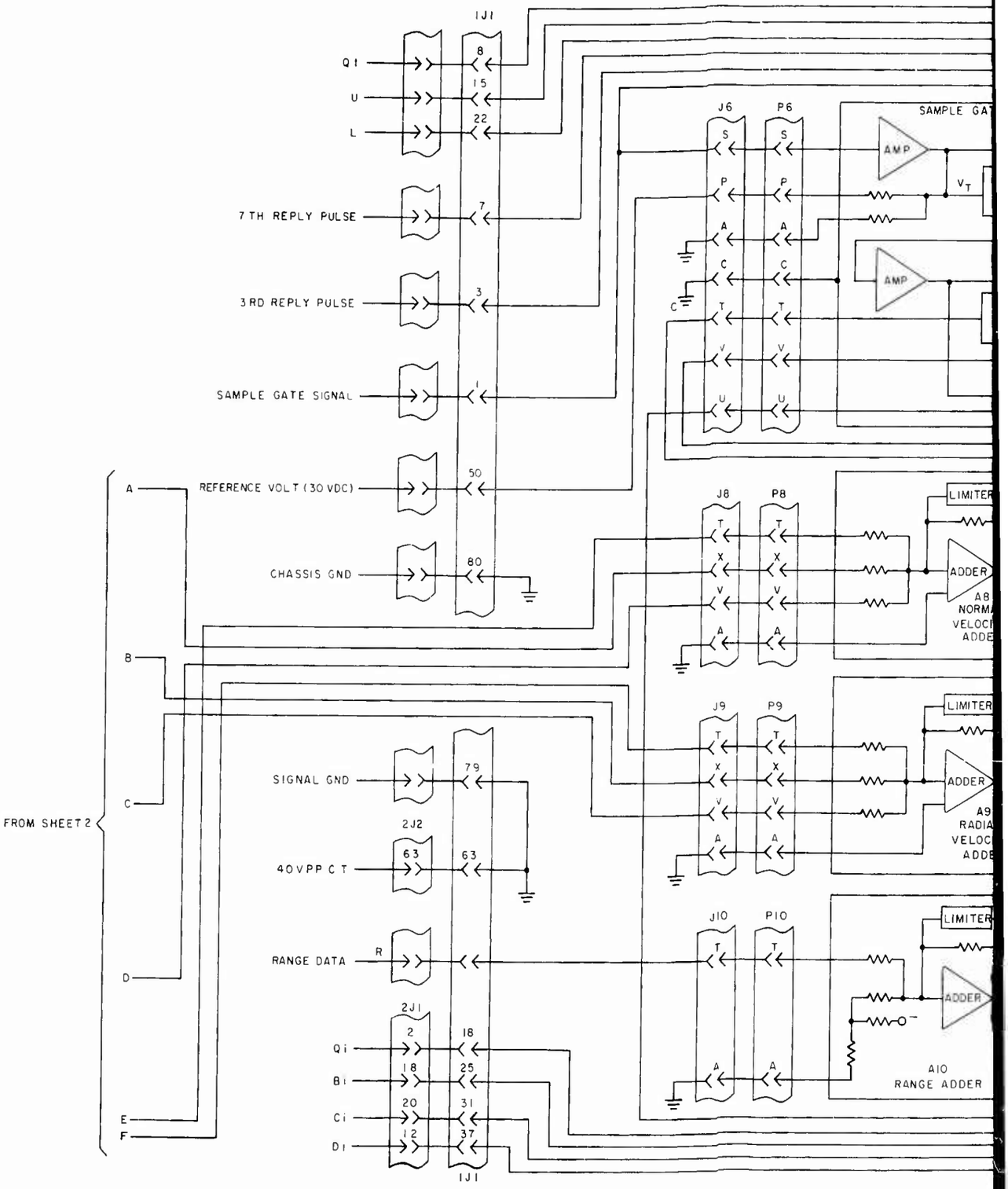

J5
P5
A5K1
+VNB
-VNB
+VEB
-VEB
P5
J5
U
V
W
X
26V
400 ~
J4
P4
A4
MAGNETIC
BEARING
SERVO
C1
ORN
BLU
WH
YEL
WH-RD
WH-BLK
RD
BLK
RD
BLK
M
G
C.T.
2121:1
θ+θc ta = θ
P2
SIN
COS
POT
P1
J1
1K2
CLAMP
CLAMP
30 VDC
UNFIL.
BRN
GRN
BLK
BLU
YEL



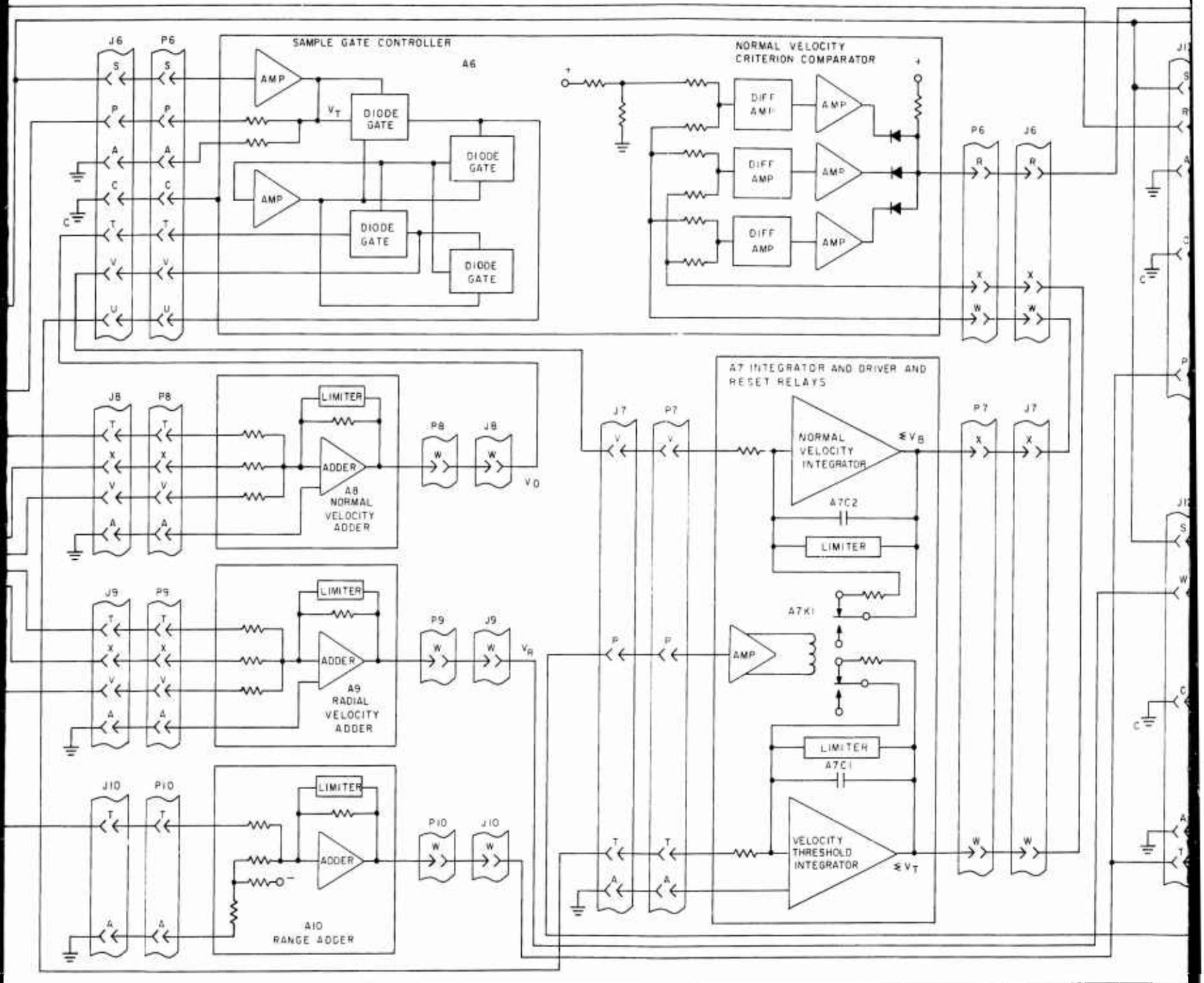
3

FIGURE 5-5

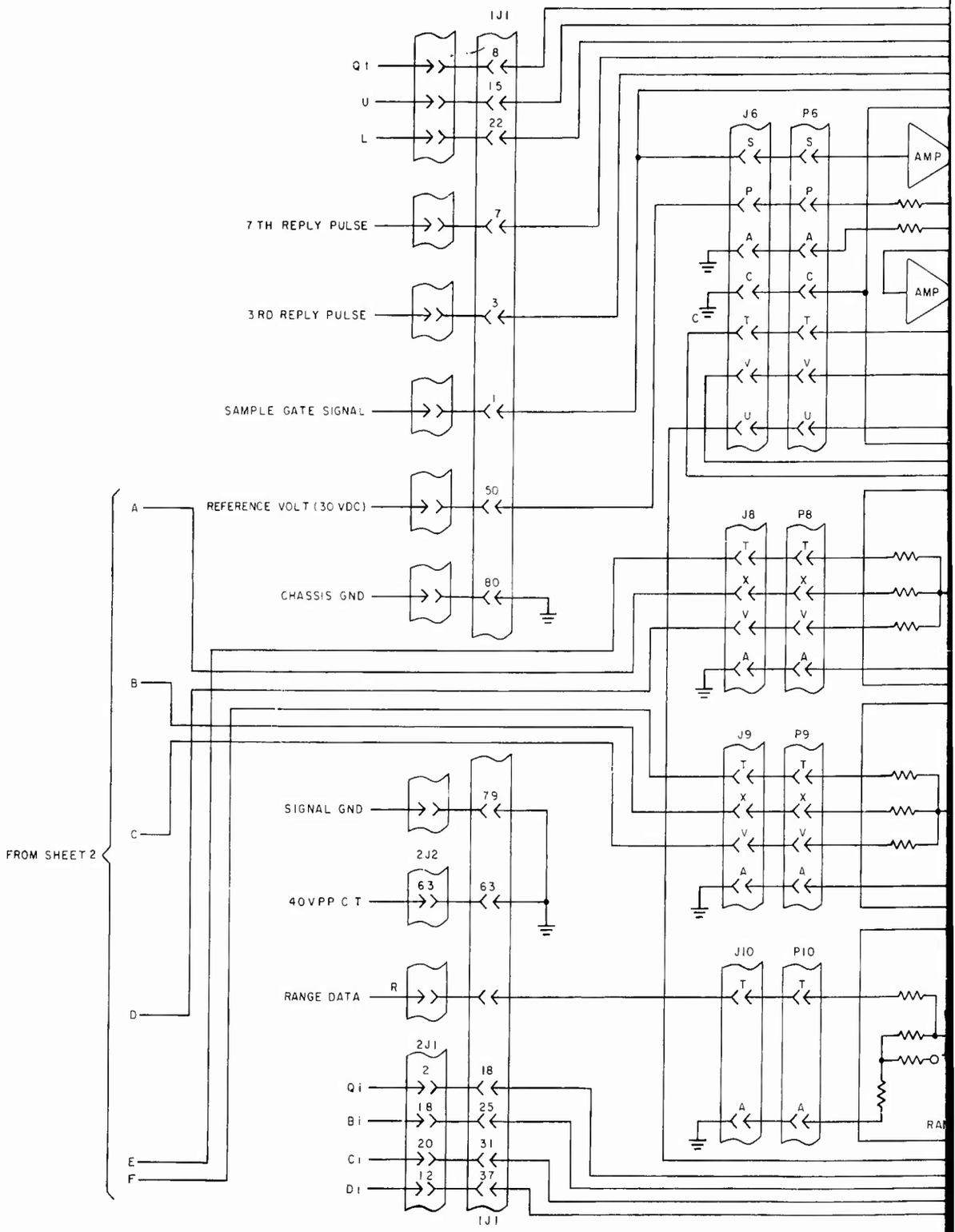
INTERROGATOR COMPUTER SIGNAL SCHEMATIC
(SHEET 2 OF 4)


1J1
Q1
U
L
7TH REPLY PULSE
3RD REPLY PULSE
SAMPLE GATE SIGNAL
REFERENCE VOLT (30 VDC)
CHASSIS GND
SIGNAL GND
40 VPP C T
RANGE DATA
2J1
2J2
FROM SHEET 2
A
B
C
D
E
F
J6
P6
SAMPLE GAT
AMP
J8
P8
LIMITER
ADDER
A8
NORMA
VELOCI
ADDE
J9
P9
A9
RADIA
VELOC
ADDE
J10
P10
A10
RANGE ADDER

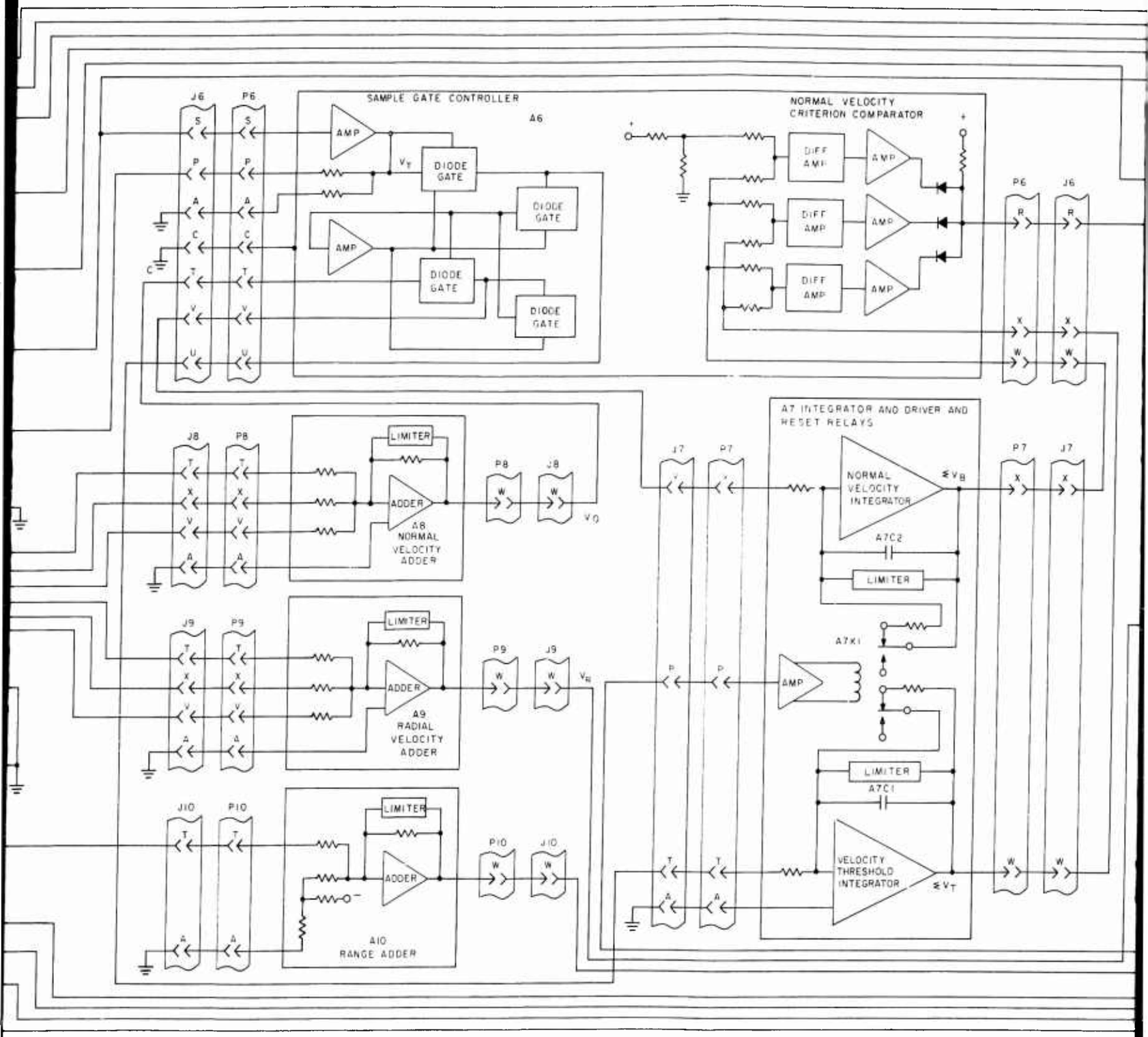
1

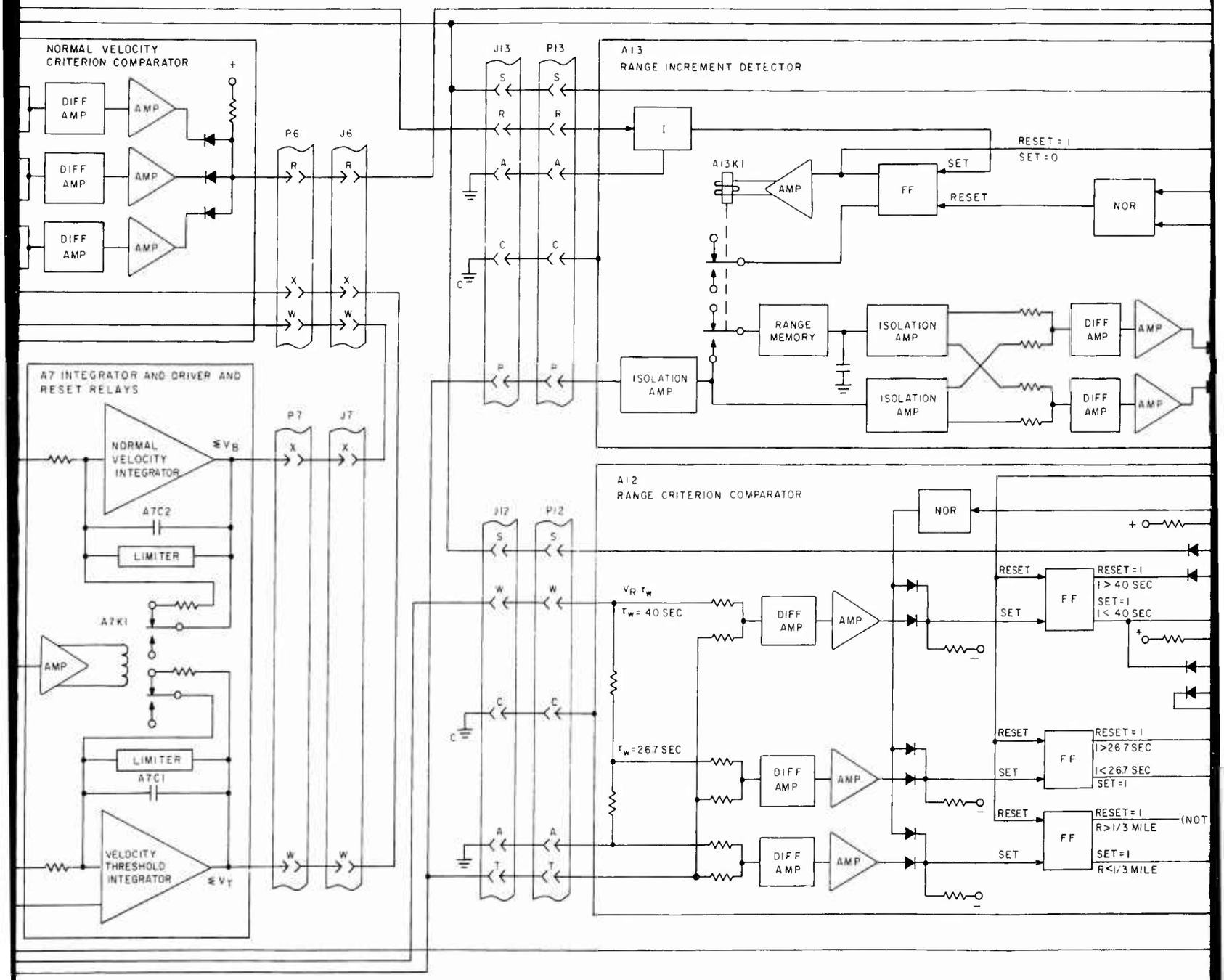

SAMPLE GATE CONTROLLER
A6
AMP
DIODE GATE
NORMAL VELOCITY CRITERION COMPARATOR
DIFF AMP
A8 NORMAL VELOCITY ADDER
A9 RADIAL VELOCITY ADDER
A10 RANGE ADDER
LIMITER
ADDER
A7 INTEGRATOR AND DRIVER AND RESET RELAYS
NORMAL VELOCITY INTEGRATOR
VELOCITY THRESHOLD INTEGRATOR
A7C2
A7C1
A7K1

2


1J1
Q1
U
L
8
15
22
7TH REPLY PULSE
7
3RD REPLY PULSE
3
SAMPLE GATE SIGNAL
1
REFERENCE VOLT (30 VDC)
50
CHASSIS GND
80
SIGNAL GND
79
2J2
40VPP C T
63
63
RANGE DATA
R
2J1
Qi
Bi
Ci
Di
2
18
18
25
20
31
12
37
1J1
FROM SHEET 2
A
B
C
D
E
F
J6
P6
J8
P8
J9
P9
J10
P10
AMP
AMP
RAN

1


SAMPLE GATE CONTROLLER
A6
AMP
DIODE GATE
NORMAL VELOCITY CRITERION COMPARATOR
DIFF AMP
A8 NORMAL VELOCITY ADDER
A9 RADIAL VELOCITY ADDER
A10 RANGE ADDER
LIMITER
ADDER
A7 INTEGRATOR AND DRIVER AND RESET RELAYS
NORMAL VELOCITY INTEGRATOR
VELOCITY THRESHOLD INTEGRATOR
A7C2
A7C1
A7K1


NORMAL VELOCITY CRITERION COMPARATOR
DIFF AMP
AMP
P6
J6
J13
P13
A13
RANGE INCREMENT DETECTOR
A13K1
SET
RESET
RESET = 1
SET = 0
NOR
RANGE MEMORY
ISOLATION AMP
A7 INTEGRATOR AND DRIVER AND RESET RELAYS
NORMAL VELOCITY INTEGRATOR
A7C2
LIMITER
A7K1
A7C1
VELOCITY THRESHOLD INTEGRATOR
P7
J7
J12
P12
A12
RANGE CRITERION COMPARATOR
τ_w = 40 SEC
τ_w = 26.7 SEC
I > 40 SEC
I < 40 SEC
SET = I
I > 26.7 SEC
I < 26.7 SEC
R > 1/3 MILE
R < 1/3 MILE

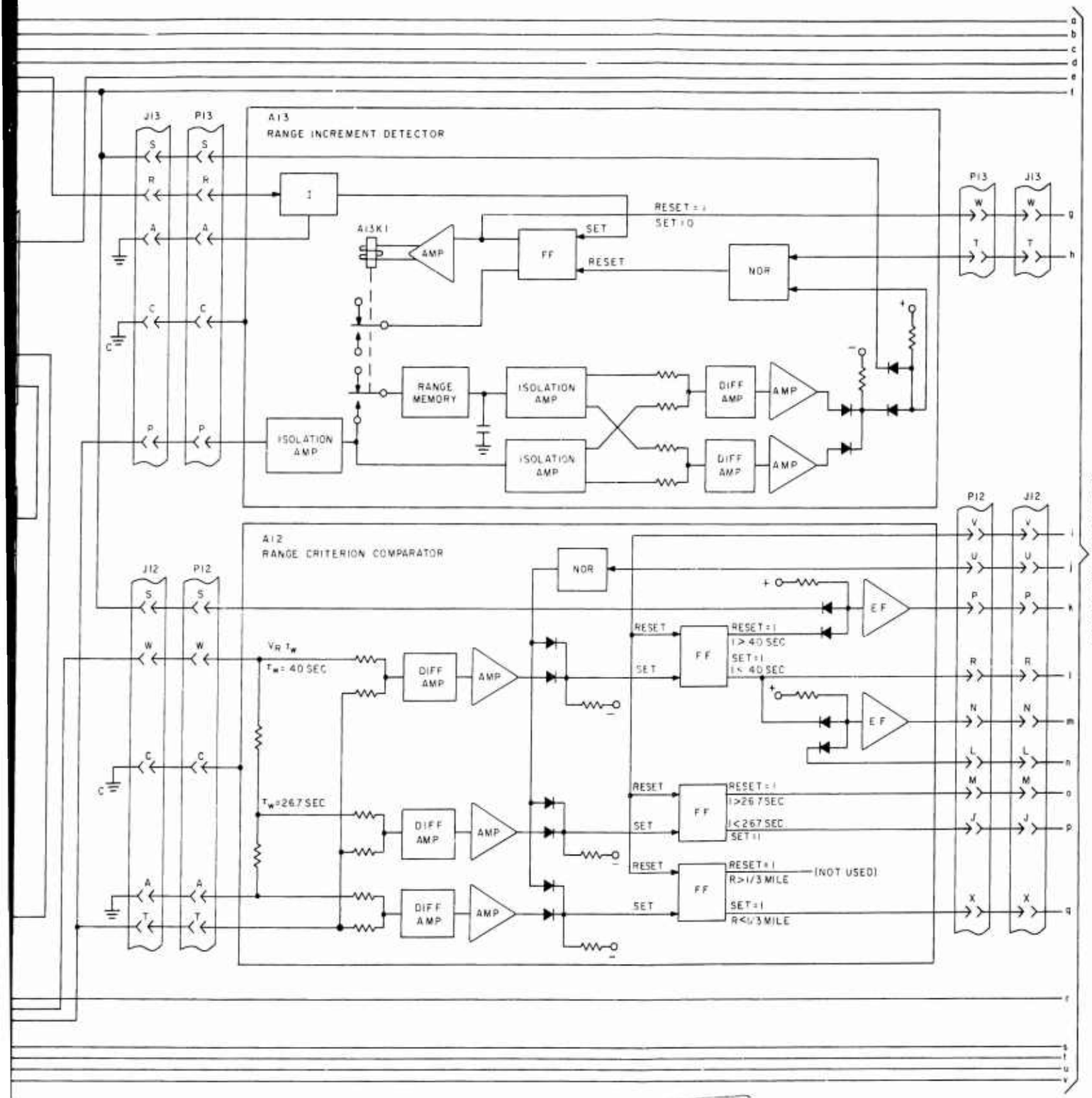
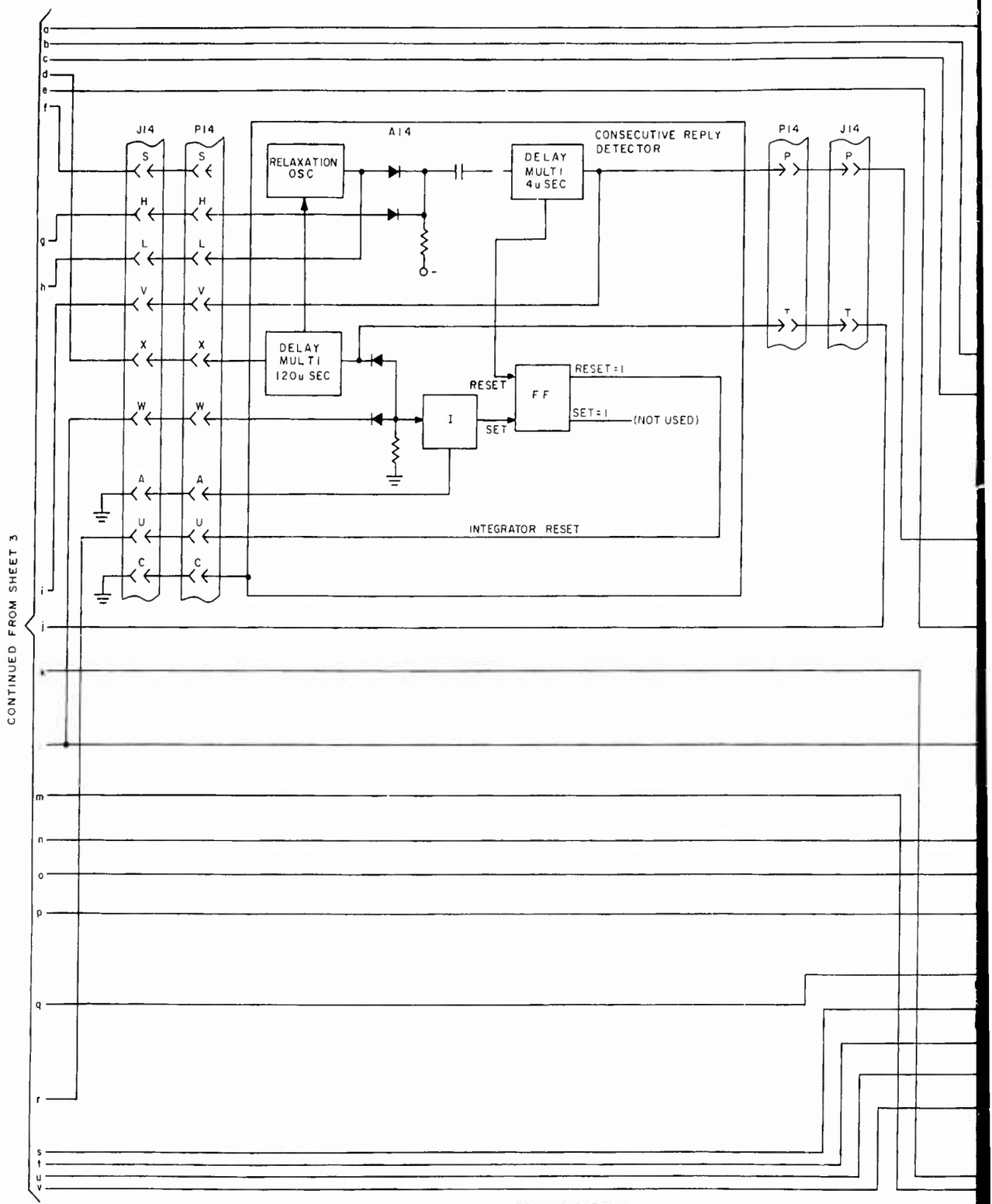


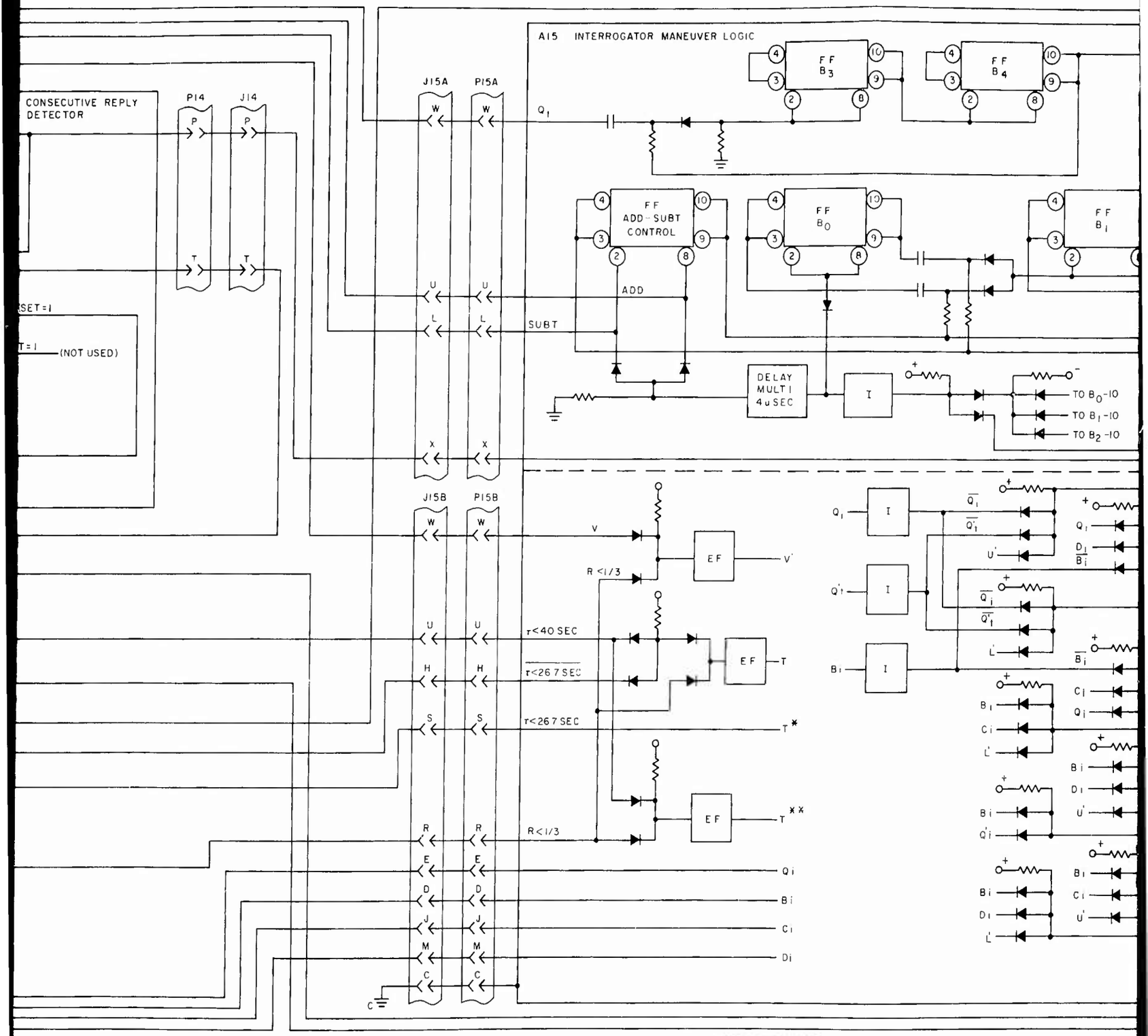
FIGURE 5-5

INTERROGATOR COMPUTER SIGNAL SCHEMATIC
(SHEET 3 OF 4)

4


CONTINUED FROM SHEET 3
J14
P14
A14
CONSECUTIVE REPLY DETECTOR
P14
J14
RELAXATION OSC
DELAY MULTI 4u SEC
DELAY MULTI 120u SEC
RESET
SET
I
FF
RESET=1
SET=1
(NOT USED)
INTEGRATOR RESET
S
H
L
V
X
W
A
U
C
P
T
a
b
c
d
e
f
g
h
i
j
k
m
n
o
p
q
r
s
t
u
v

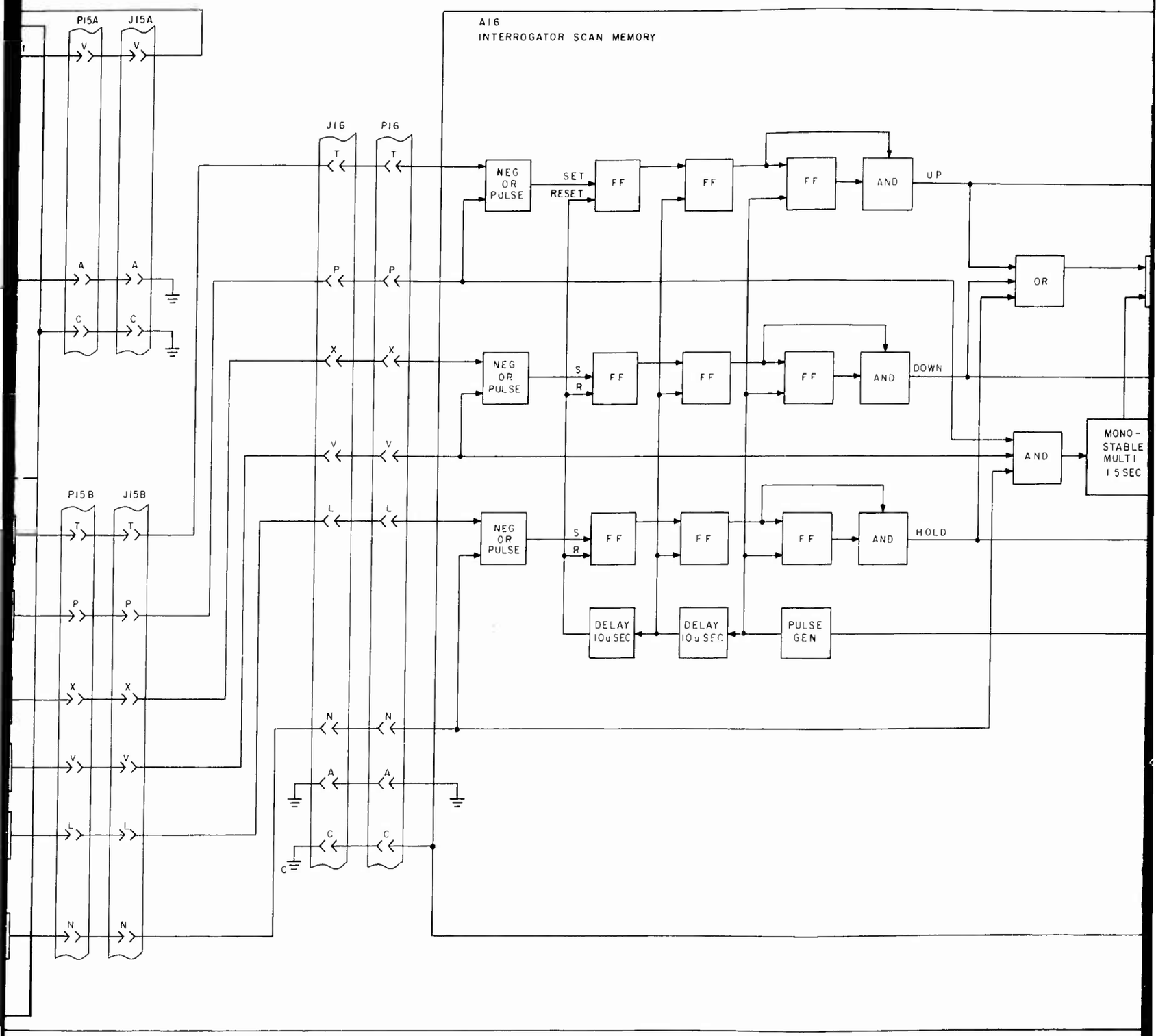
1


A15 INTERROGATOR MANEUVER LOGIC
CONSECUTIVE REPLY DETECTOR
P14
J14
J15A
P15A
J15B
P15B
FF B3
FF B4
FF ADD-SUBT CONTROL
FF B0
FF B1
ADD
SUBT
DELAY MULTI 4 u SEC
TO B0-10
TO B1-10
TO B2-10
EF
τ<40 SEC
τ<26.7 SEC
R<1/3
(NOT USED)

2

FF B3
FF B4
FF B0
FF B1
FF B2
Q't
U'
L'
Z
P15A
J15A
J16
P16
I
AMP
TO B0-10
TO B1-10
TO B2-10
TO B0-4
TO B1-4
TO B2-4
TO B3-10
TO B4-10
EF
P15B
J15B

3


A16
INTERROGATOR SCAN MEMORY
P15A
J15A
J16
P16
P15B
J15B
NEG OR PULSE
SET
RESET
FF
AND
UP
OR
DOWN
MONO-STABLE MULTI 1.5 SEC
HOLD
DELAY 10u SEC
PULSE GEN

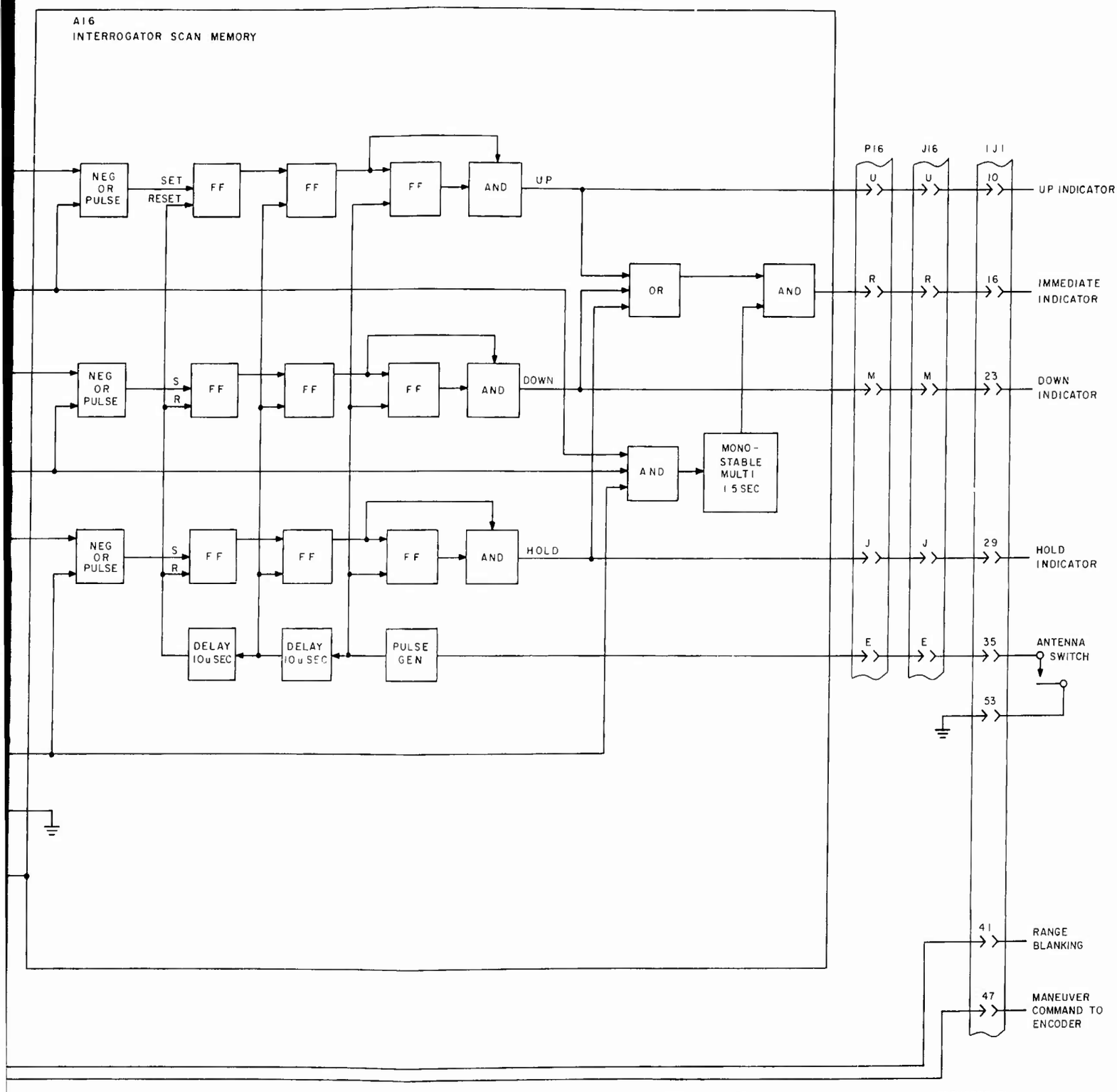


FIGURE 5-5

INTERROGATOR COMPUTER SIGNAL SCHEMATIC
(SHEET 4 OF 4)

Reset of the velocity integrators is controlled by the flip-flop in the integrator reset circuits which is set whenever a reply is received for which the derived time-to-close is less than 40 seconds. This input is inhibited until 120 microseconds after the receipt of the last reply pulse to assure that derived time-to-close has reached steady state. Reset stimuli are obtained from the range increment detector and the consecutive reply detector, described below.

The consecutive reply detector contains a relaxation oscillator having a period of more than two interrogation intervals (more than 10 milliseconds). Completion of the relaxation cycle produces an integrator reset output. The oscillator is recycled by each sample gate, thus inhibiting an output unless two consecutive sample gates are missing.

In the range increment detector, the range derived from the first reply from an intruder is stored in a range memory. Further inputs to the memory are inhibited about one millisecond after the receipt of the third reply pulse, the delay being inherent in the relay which does the switching. The circuit is reset either by an output from the consecutive reply detector or an output from the differential amplifiers in the range increment detector, indicating the receipt of a range sample which differs by more than 0.36 nautical miles from the stored sample. Resetting the range increment circuits also produces an integrator reset output.

The function of the Maneuver Logic is to determine the type of avoidance maneuver to be made by the interrogator aircraft based on the specified maneuver rules. These rules are defined in paragraph 8.0 of the interrogator characteristics.[6] The output of the maneuver logic elements consists of a pulse appearing on one of six wires indicating one of the six possible maneuvers. The logic equations, that must be satisfied to provide each of the six outputs are as follows:

$$P_{up} = 2TV\,(\bar{Q}_i\,\bar{Q}_t\,U + A_i\,D_i)$$

$$I_{up} = 2T^{*}V\,(\bar{Q}_i\,\bar{Q}_t\,U + A_i\,D_i)$$

$$R_{down} = 2TV\,(\bar{Q}_i\,\bar{Q}_t\,L + A_i\,C_i$$

$$I_{down} = 2T^{*}V\,(\bar{Q}_i\,\bar{Q}_t\,L + A_i\,C_i)$$

$$R_{hold} = 2T^{**}V\,(B_i\,C_i\,L + B_i\,D_i\,U + B_i\,Q_t)$$

$$I_{hold} = 2T^{**}V\,(B_i\,C_i\,U + B_i\,D_i\,L)$$

- - - - - - -

[6] Design Study Report - Experimental Evaluation of Compatible PWI/CAS Interrogator-Transponder Techniques, Volume II, furnished by Sperry Gyroscope Company to the Federal Aviation Agency under Contract No. FAA/ARDS-444.

The symbol definitions for the preceding equations are as follows:

V = normal velocity criterion satisfied

T = 27.6 sec $\leq \tau \leq$ 40 sec, where τ = time to closest approach

T* = τ < 26.7 sec

T** = τ < 40 sec R < 1 nautical mile

Q = absolute altitude rate is greater than 1350 ft/min

C = climbing

D = descending

U = interrogator is in transponder's upper altitude guard band

L = interrogator is in transponder's lower altitude guard band

R = maneuver

I = immediate maneuver

A = absolute value of altitude rate greater than 1350 ft/min., less than 3000 ft/min

B = absolute value of altitude rate greater than 3000 ft/min

Z = read in data to scan memory (computation completed).

NOTE: The suffix t or i affixed to the preceding literal terms indicates that the logical term applies to the transponder or to the interrogator respectively.

The logic operations performed in the Maneuver Logic are self-explanatory upon study of figure 5-5. The only part of the Maneuver Logic section requiring any amplification is the averaging circuit. The function of this circuit is to satisfy the requirement that the indicated direction of an up or down maneuver be based on an instantaneous average of the decoded relative altitude data. A second function is to inhibit a transponder climbing or descending conclusion unless two or more samples of this code have been received. The method used is to provide an up-down counter (add-subtract) to derive the instantaneous average and a counter of two (with suitable gating logic) to provide recognition of the presence of two or more transponder climbing or descending codes.

The scan memory provides the following functions:

- inhibits warnings unless collision decisions are made on two successive scans
- serves as a "data hold" to provide a continuous rather than intermittent display.

Each command channel (up, down, or hold) of the memory is identical and consists of a shift register which is advanced once each scan by shift pulses from the antenna switch. A command is indicated if both of the last two stages are in the set condition. If any input on a scan has an immediate label, a monostable multivibrator with a period of 1.5 seconds is also triggered. Its output is gated out as an "immediate" indication concurrently with the maneuver command. Because the multivibrator period is shorter than the scan cycle, an intermittent "immediate" indication is produced.

6. Transponder Computer

The transponder computer converts heading, altitude, and altitude rate data to a form suitable for coding and decoding and contains the logic necessary to provide the intelligence for the limited transponder maneuver display. A signal schematic is shown in figure 5-6.

The heading servo resolves the transponding aircraft's airspeed into north and east components and contains a quadrant switch to produce binary data on their polarities. A lag network has been included in the error sensor to make the servo an effective low-pass filter, resulting in a shaft position proportional to the average heading. The control transformer output voltage, however, will contain the high-frequency variation. This signal is used in the relative bearing servo (in the interrogator collision computer) to cancel the high frequency component of train angle. The limiting diode in the generator feedback circuit is used to allow faster slewing than would be otherwise possible for large errors in heading. This feature permits quicker recovery from the effects of turns.

The Transponder Maneuver Logic contains the logic elements necessary to determine the type of maneuver (hold or immediate hold), the data holds necessary to provide continuous displays, and provisions to establish precedence for "immediate" commands. The operation of the basic logic elements is self-explanatory. Data holds consist of flip-flops which are set by the commands and reset by relaxation oscillators having periods in excess of the antenna scan period. Each received command recycles the relaxation oscillators, thus inhibiting reset signals as long as maneuver commands continue to be received. A set condition of the "immediate" data hold inhibits further set inputs to the normal data hold, achieving the precedence function.

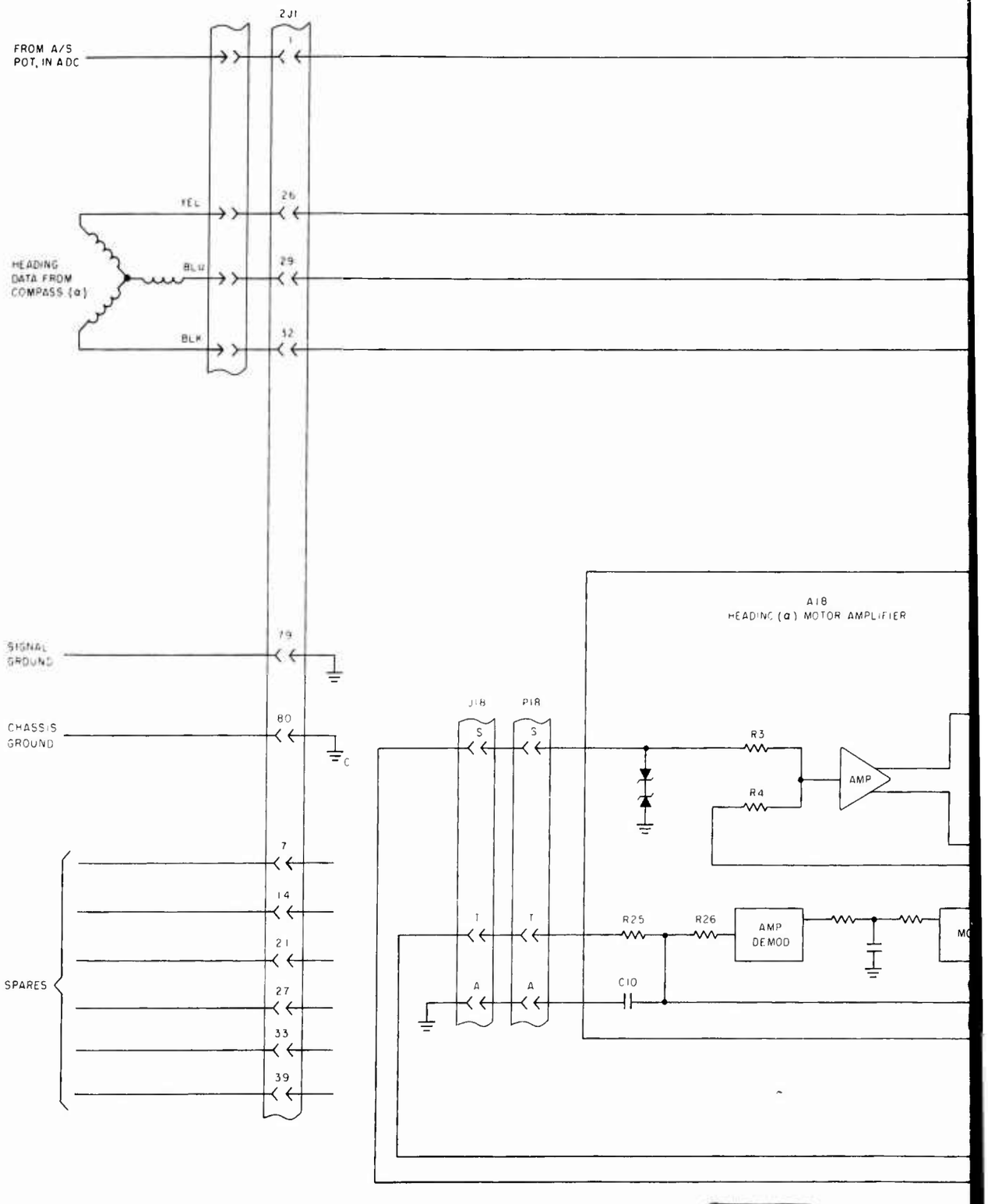
B. SUGGESTED MODIFICATIONS

In the course of the evaluation program. circuit modifications suggested themselves. These modifications have the potential of improving system performance or of achieving satisfactory performance more economically. Because of the experimental nature of the program, these changes were not implemented or even explored in detail. However, the nature of these suggested changes is given for completeness.

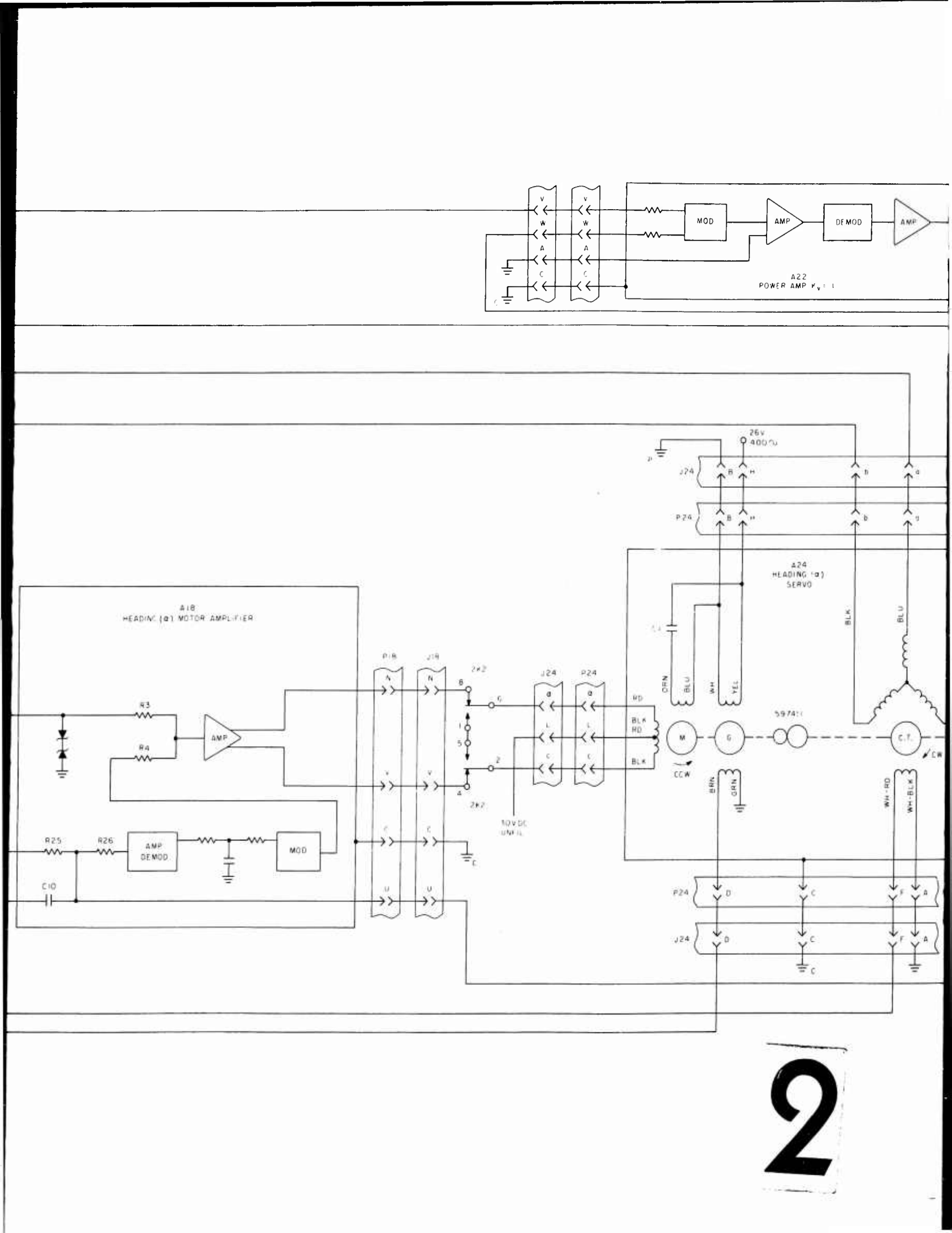
In general, an effort devoted to defining the simplest circuit to accomplish the present functions would be beneficial. For instance, the number of elements employed in logic circuits could generally be reduced, by rearrangement. A net gain might also be realized by sharing elements, such as delay lines, between functions. No effort has been devoted to such simplification beyond that intuitively done in normal engineering practices.

The sonic delay lines and associated circuits employed for encoding and, in some cases, for decoding are marginal in performance for the application. The primary deficiencies are limited bandwidth, high reflection levels, and excessive pulse generator recovery times. Improved reliability could be achieved by substituting electromagnetic delay lines. This substitution would also facilitate the sharing of elements.

The linearity of the linear sweep circuits and associated memory circuits, where employed, could be improved. The most obvious approach is to employ an operational amplifier as an integrator, as in the interrogator computer. Such an integrator could serve as both the sweep generator and memory, where required. An alternate approach would be to employ digital techniques, by counting clock pulses and converting the count to an analog output. The counter could also double as a memory where required.


2J1
FROM A/S POT, IN ADC
1
YEL
26
HEADING DATA FROM COMPASS (α)
BLU
29
BLK
32
SIGNAL GROUND
79
CHASSIS GROUND
80
SPARES
7
14
21
27
33
39
A18
HEADING (α) MOTOR AMPLIFIER
J1B
P1B
S
T
A
R3
R4
AMP
R25
R26
AMP DEMOD
C10

1


V
W
A
C
MOD
AMP
DEMOD
AMP
A22
POWER AMP K_V = 1
26V
400Cy
J24
P24
A24
HEADING (α)
SERVO
A18
HEADING (α) MOTOR AMPLIFIER
P18
J18
2K2
2K2
10V DC
UNREG
R3
R4
AMP
R25
R26
AMP
DEMOD
MOD
C10
ORN
BLU
WH
YEL
BLK
BLU
RD
BLK
RD
BLK
M
G
C.T.
CCW
CW
5974
BRN
GRN
WH-RD
WH-BLK
2

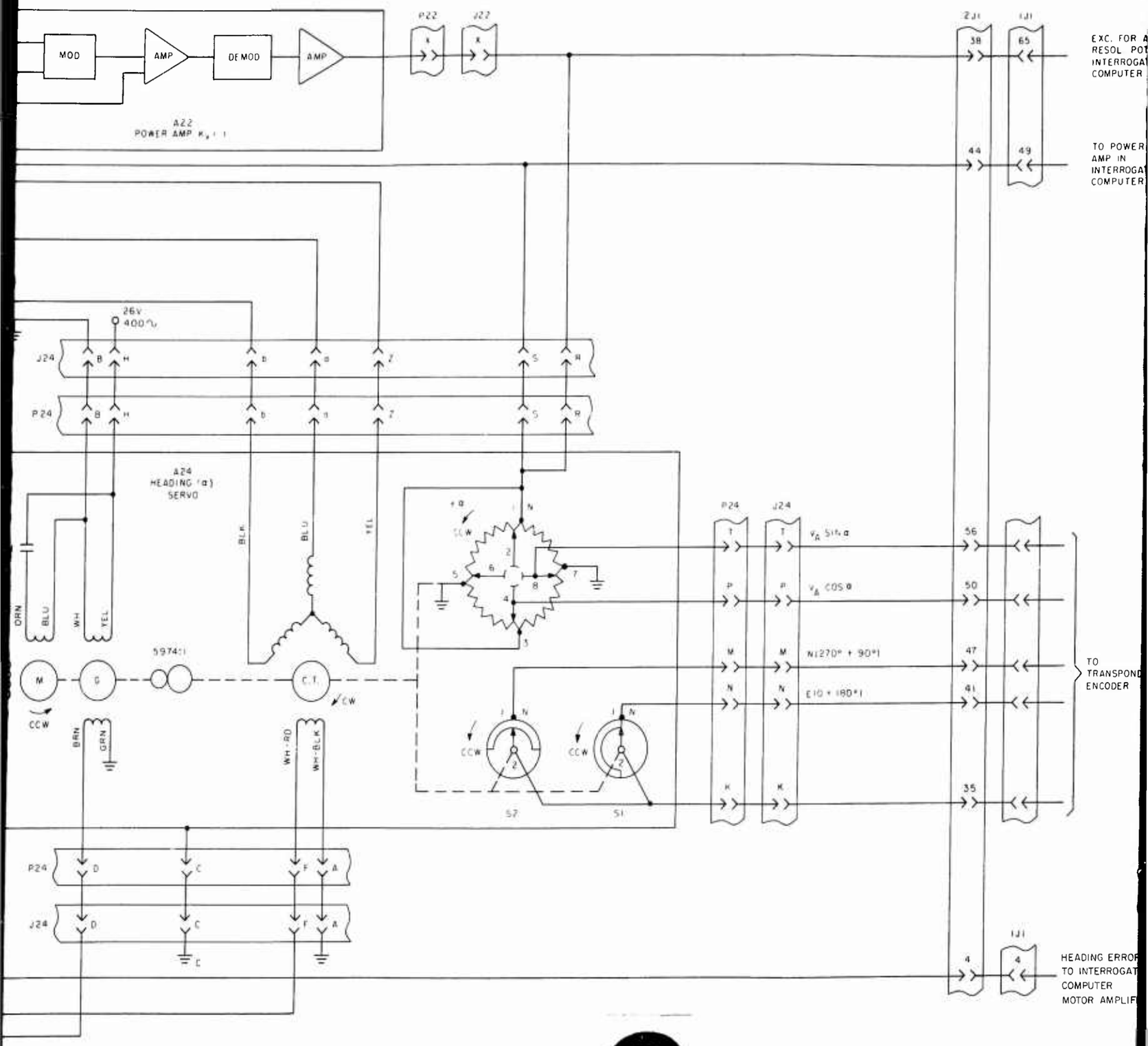


FIGURE 5-6.

TRANSPONDER COMPUTER SIGNAL SCHEMATIC (SHEET 1 OF

3

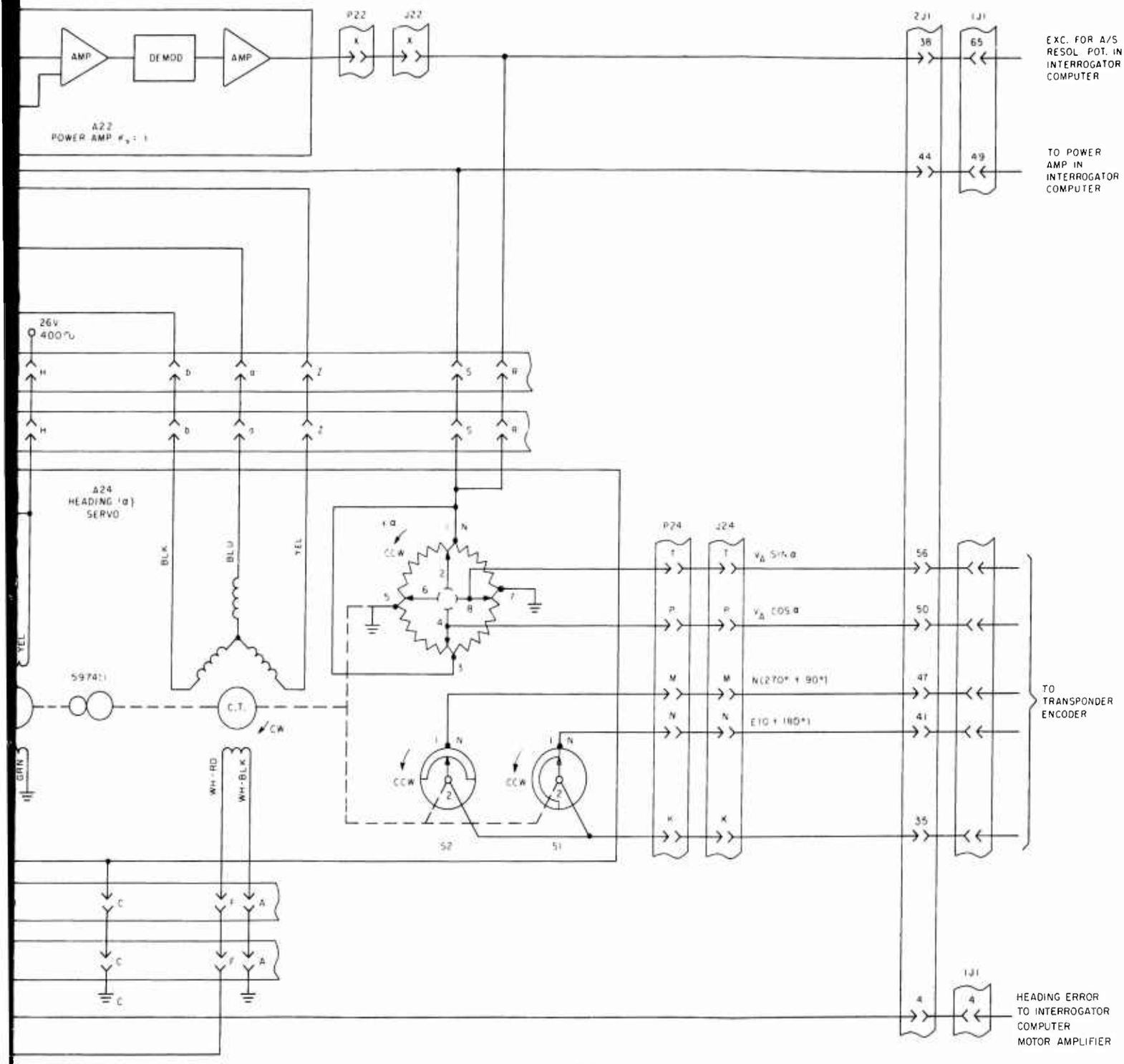
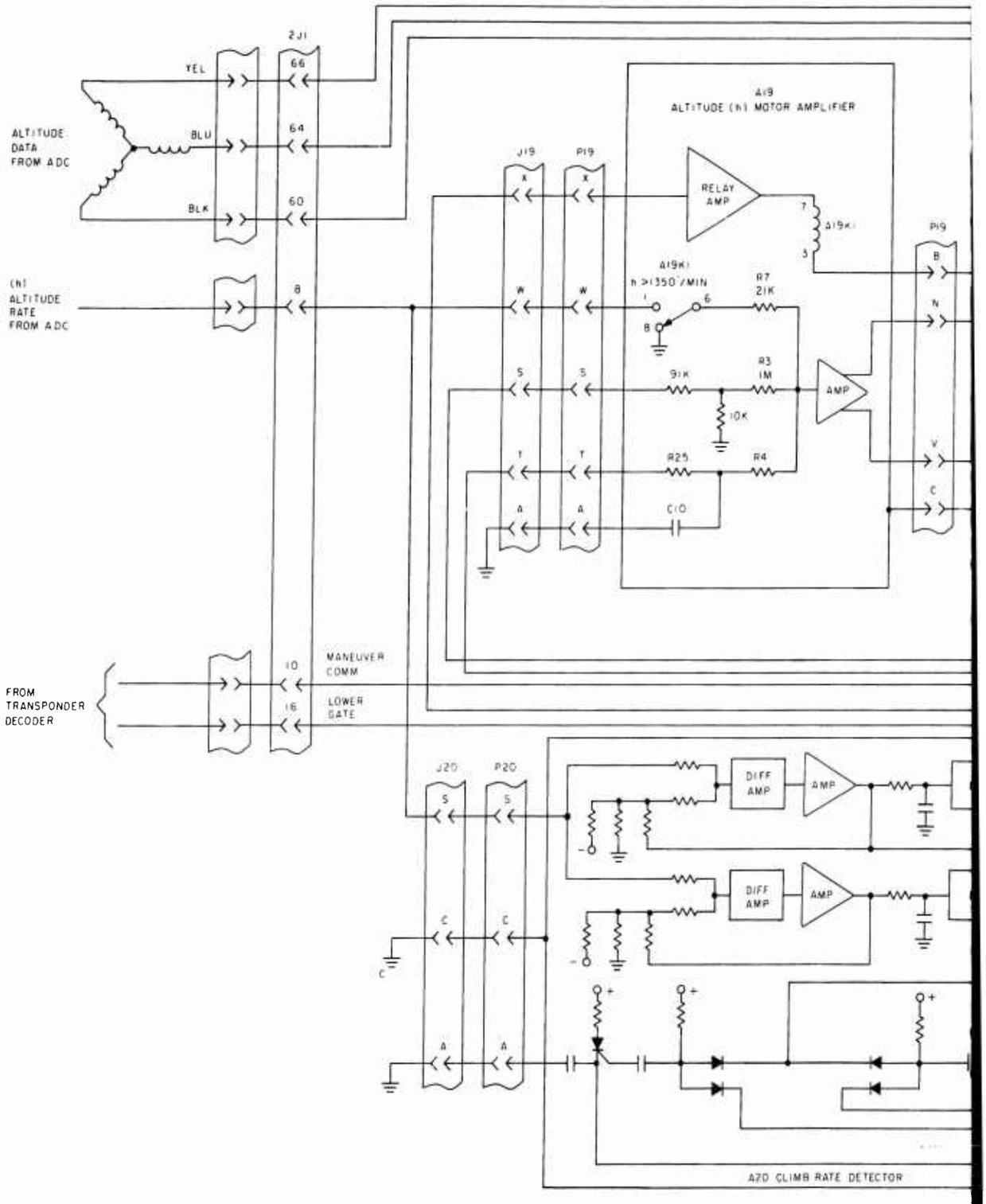
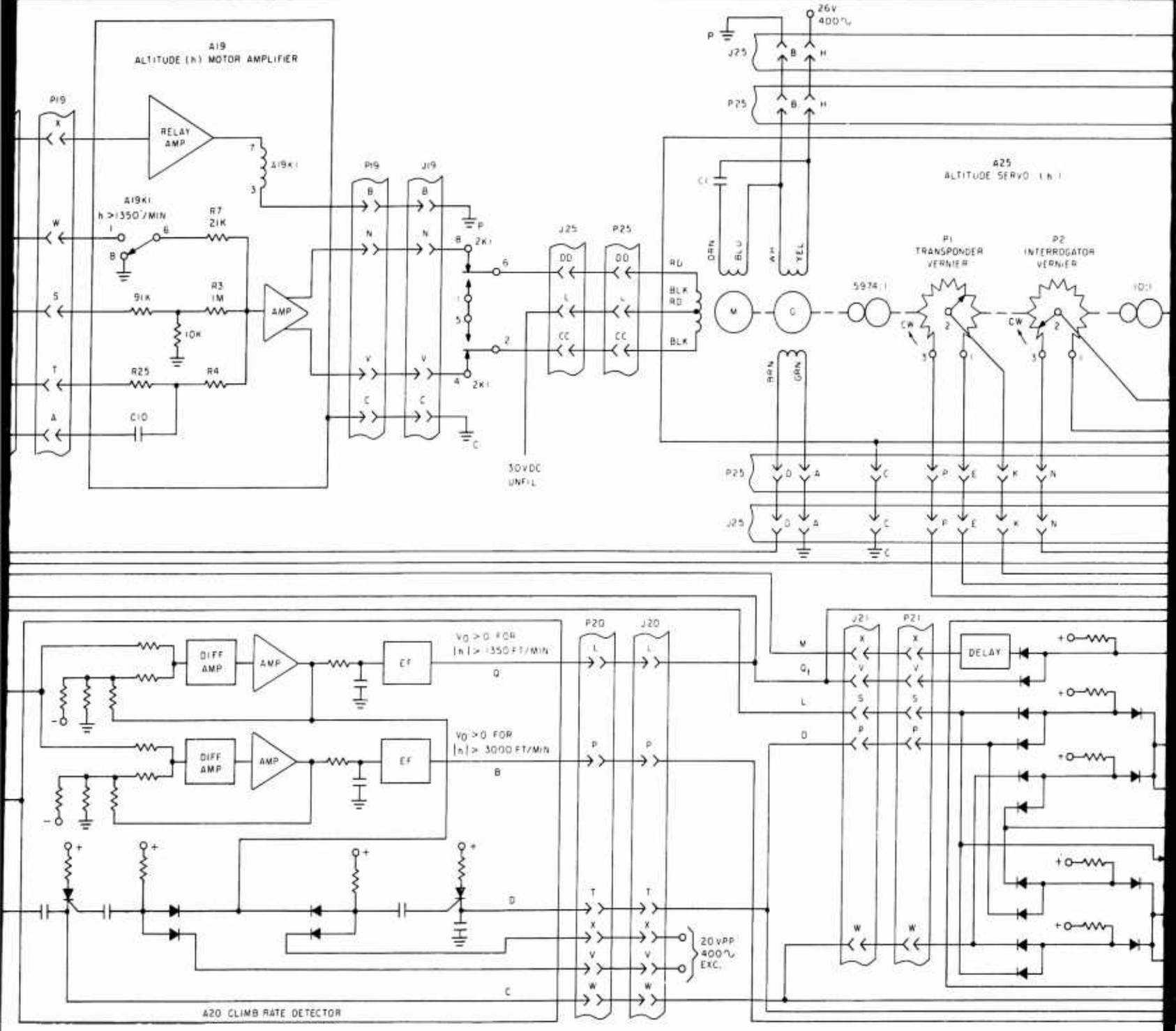


FIGURE 5-6.

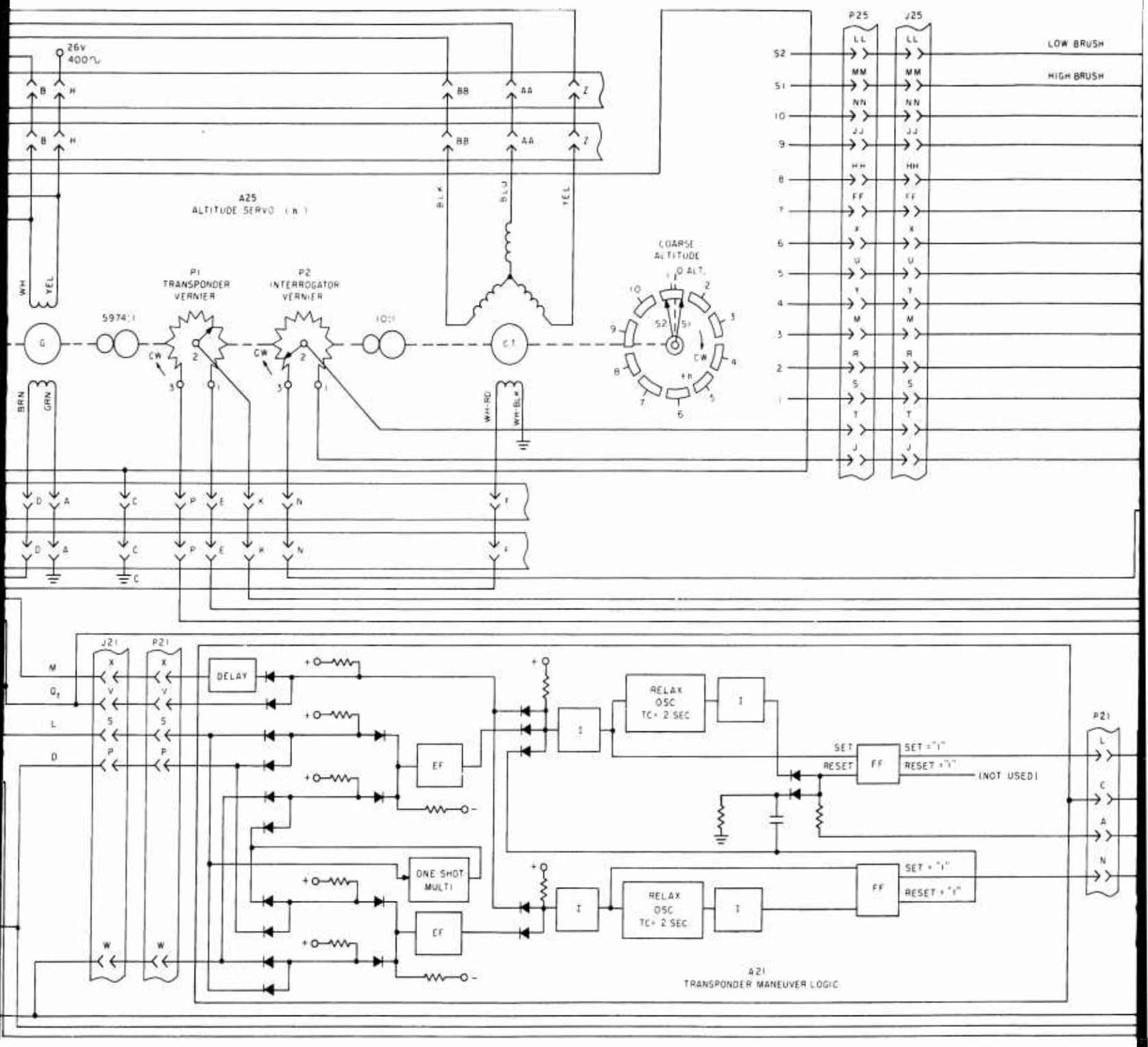
TRANSPONDER COMPUTER SIGNAL SCHEMATIC (SHEET 1 OF 2)


ALTITUDE DATA FROM ADC
YEL
BLU
BLK
J1
66
64
60
(h) ALTITUDE RATE FROM ADC
8
FROM TRANSPONDER DECODER
10
16
MANEUVER COMM
LOWER GATE
A19
ALTITUDE (h) MOTOR AMPLIFIER
J19
P19
RELAY AMP
A19K1
h >1350'/MIN
R7 21K
91K
R3 1M
10K
R25
R4
C10
AMP
J20
P20
DIFF AMP
A20 CLIMB RATE DETECTOR

1


A19
ALTITUDE (h) MOTOR AMPLIFIER
P19
RELAY AMP
A19K1
h >1350'/MIN
R7 21K
R3 1M
91K
10K
R25
R4
C10
AMP
J19
P19
2K
30VDC UNFIL
J25
P25
26V 400~
A25
ALTITUDE SERVO (h)
P1 TRANSPONDER VERNIER
P2 INTERROGATOR VERNIER
5974:1
DIFF AMP
EF
V_O >0 FOR |h| > 1350 FT/MIN
V_O >0 FOR |h| > 3000 FT/MIN
P20
J20
20 VPP 400~ EXC.
A20 CLIMB RATE DETECTOR
J21
P21
DELAY

2


26V
400~
A25
ALTITUDE SERVO (h)
P1
TRANSPONDER
VERNIER
P2
INTERROGATOR
VERNIER
COARSE
ALTITUDE
0 ALT.
P25
J25
LOW BRUSH
HIGH BRUSH
J21
P21
DELAY
EF
ONE SHOT
MULTI
RELAX
OSC
TC= 2 SEC
FF
SET
RESET
SET = "1"
RESET = "1"
(NOT USED)
A21
TRANSPONDER MANEUVER LOGIC

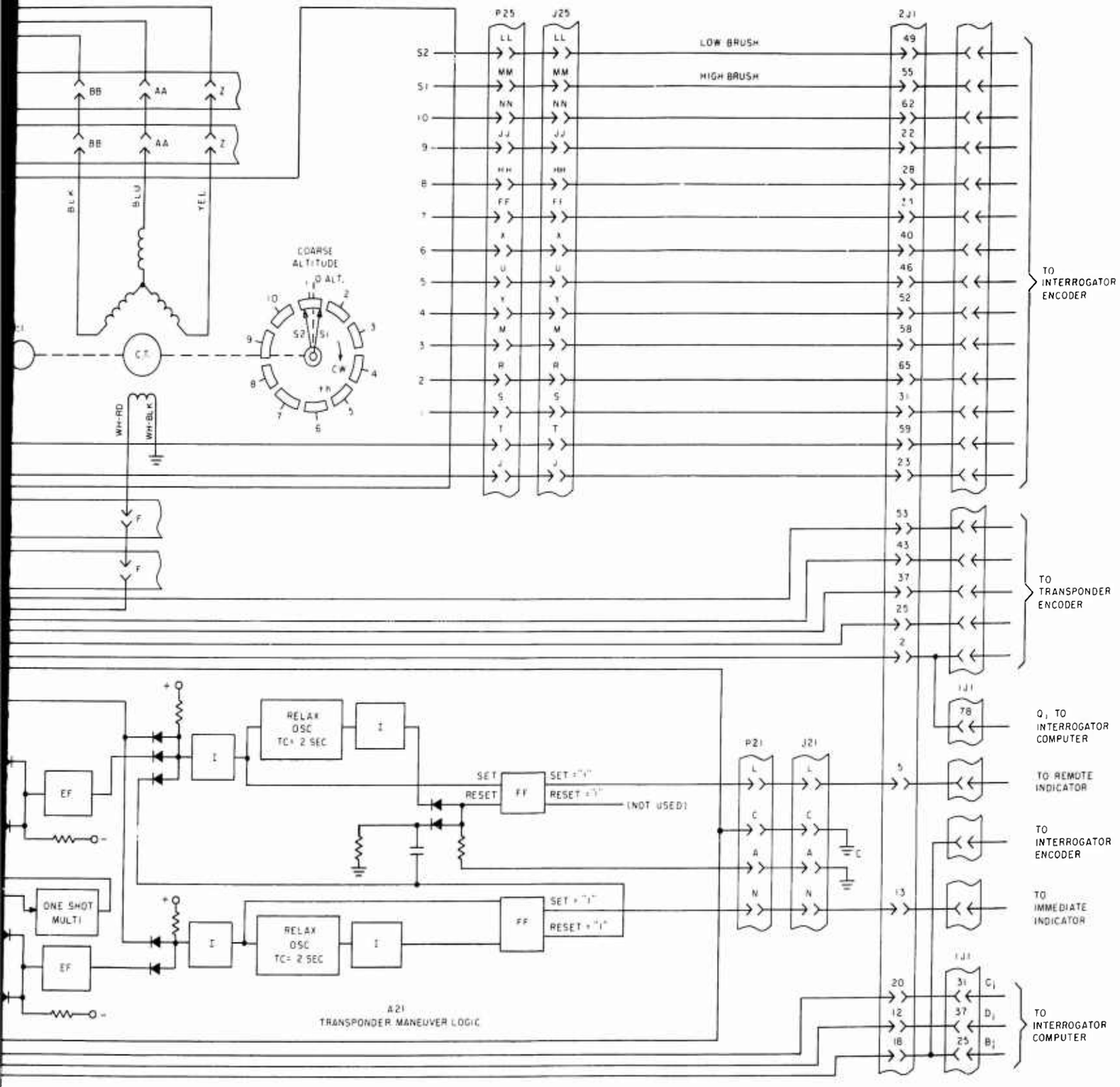
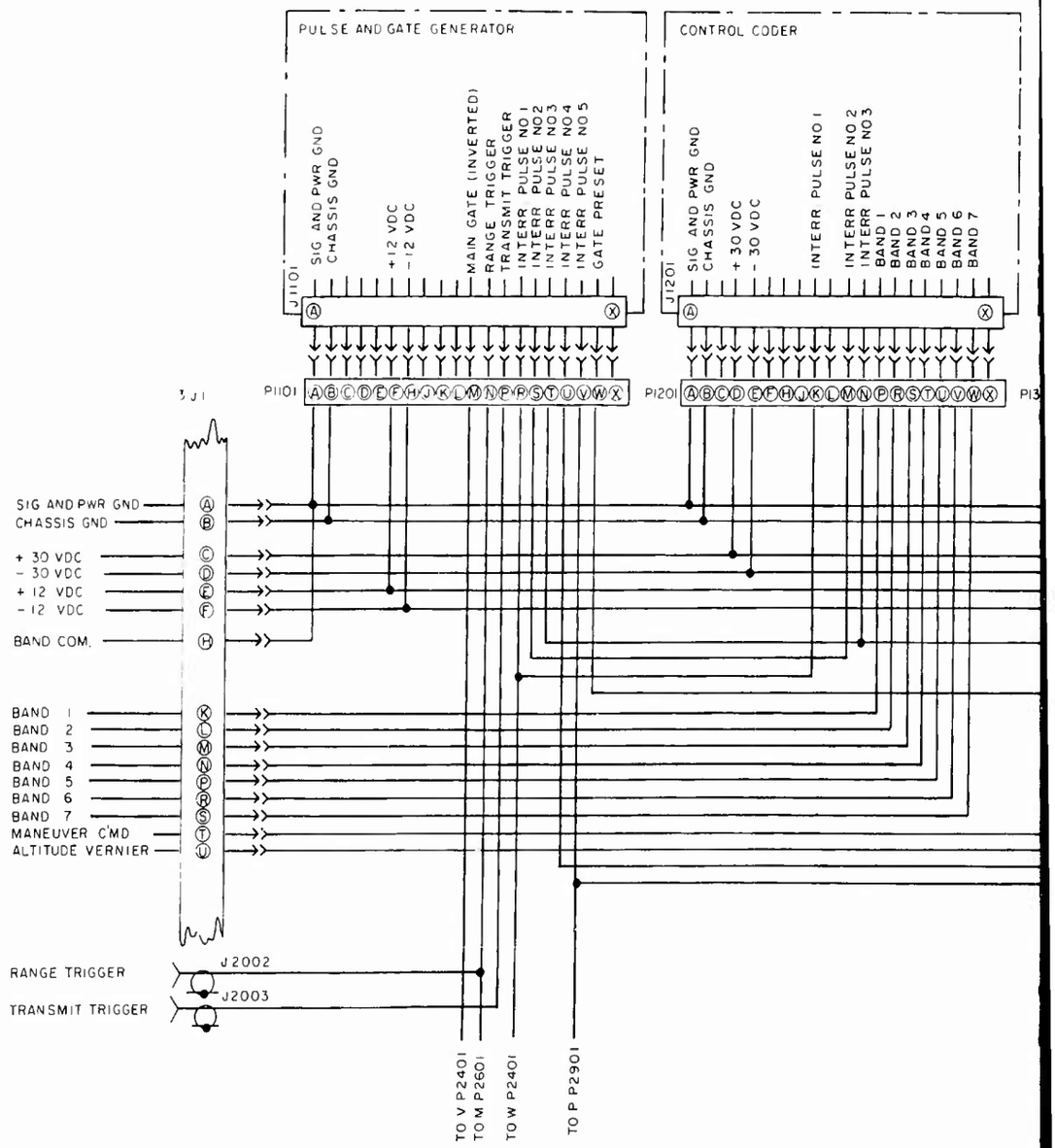


FIGURE 5-6.
TRANSPONDER COMPUTER SIGNAL SCHEMATIC (SHEET 2 OF 2)



1

INTERRO
(UNIT S

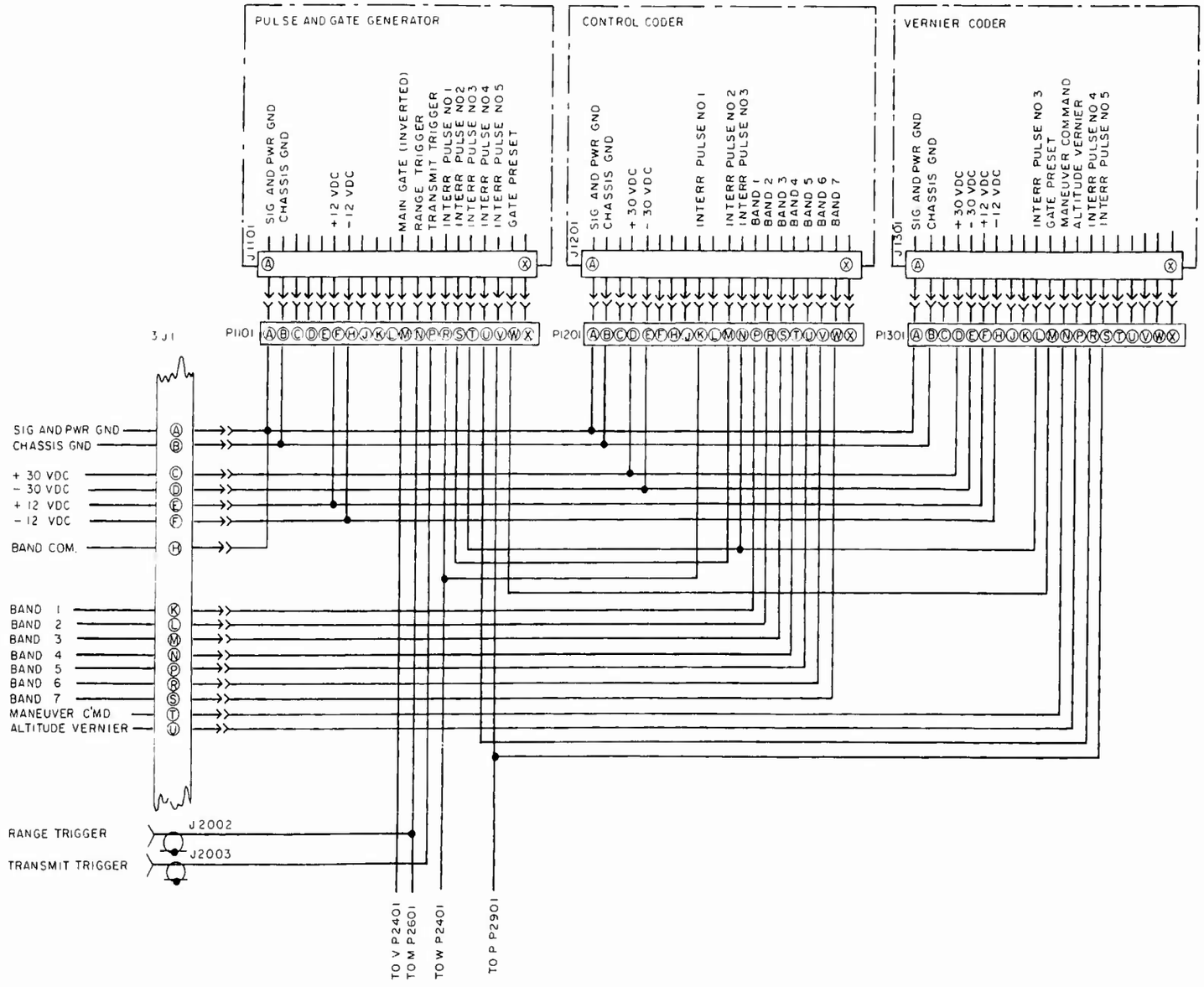
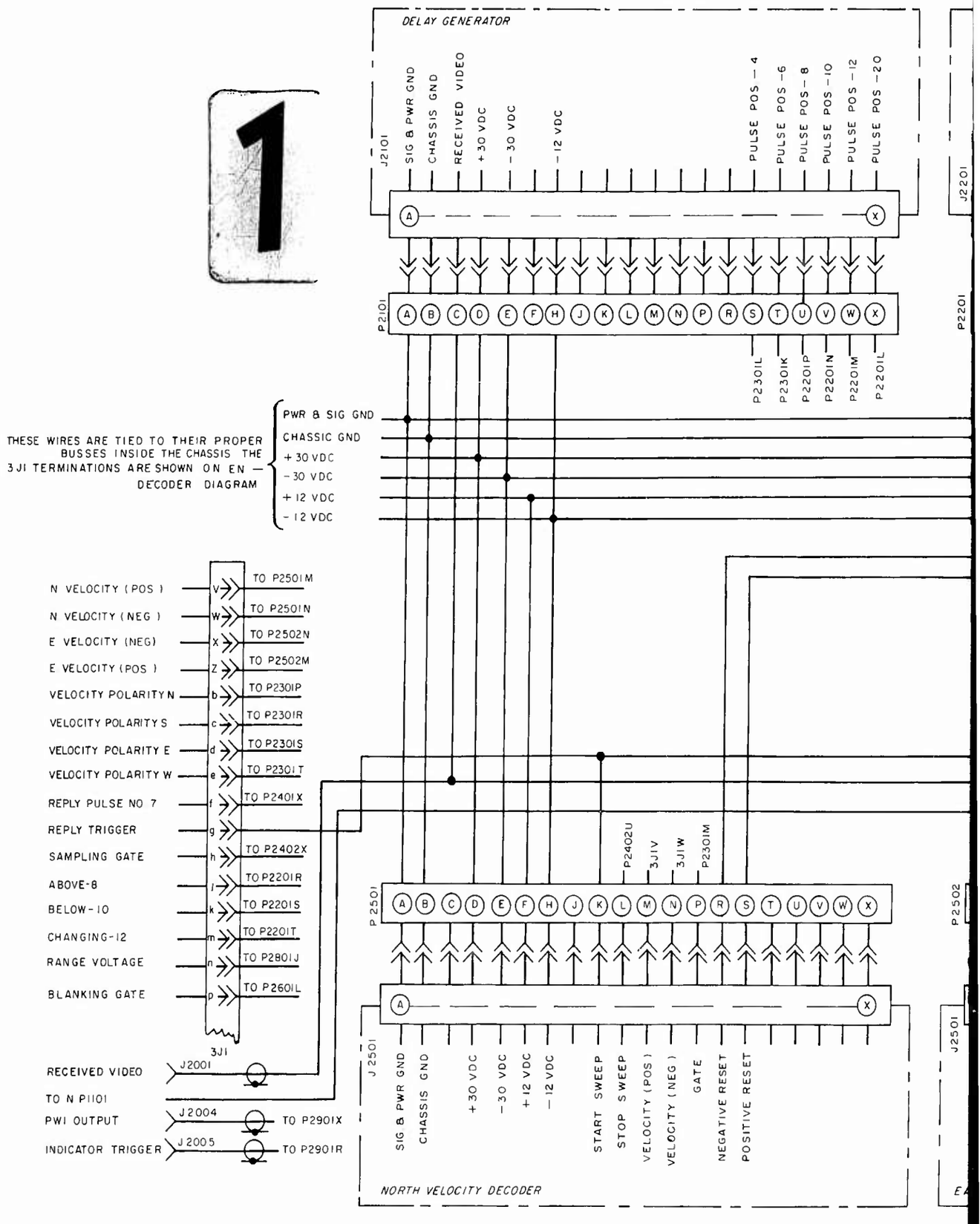
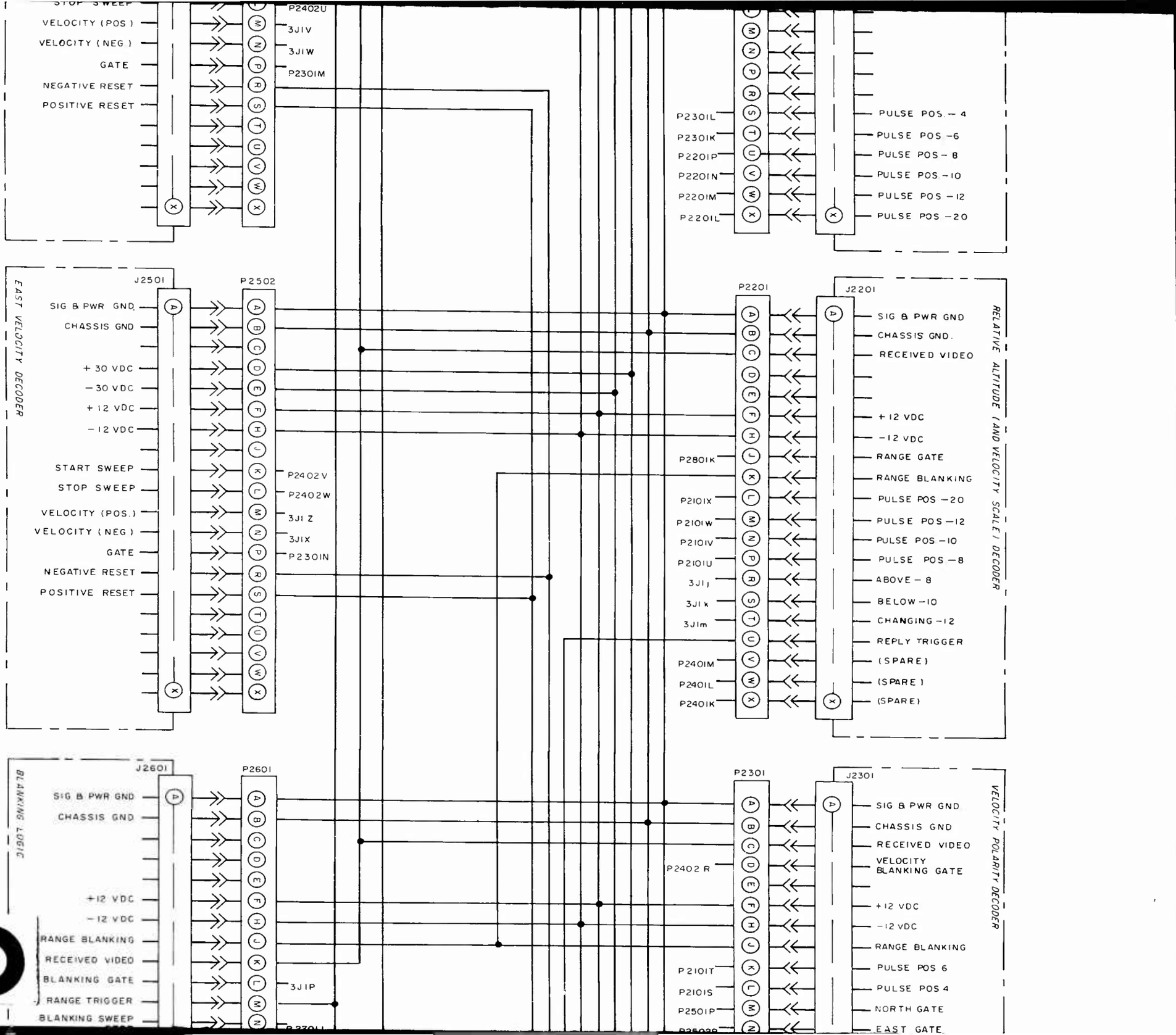
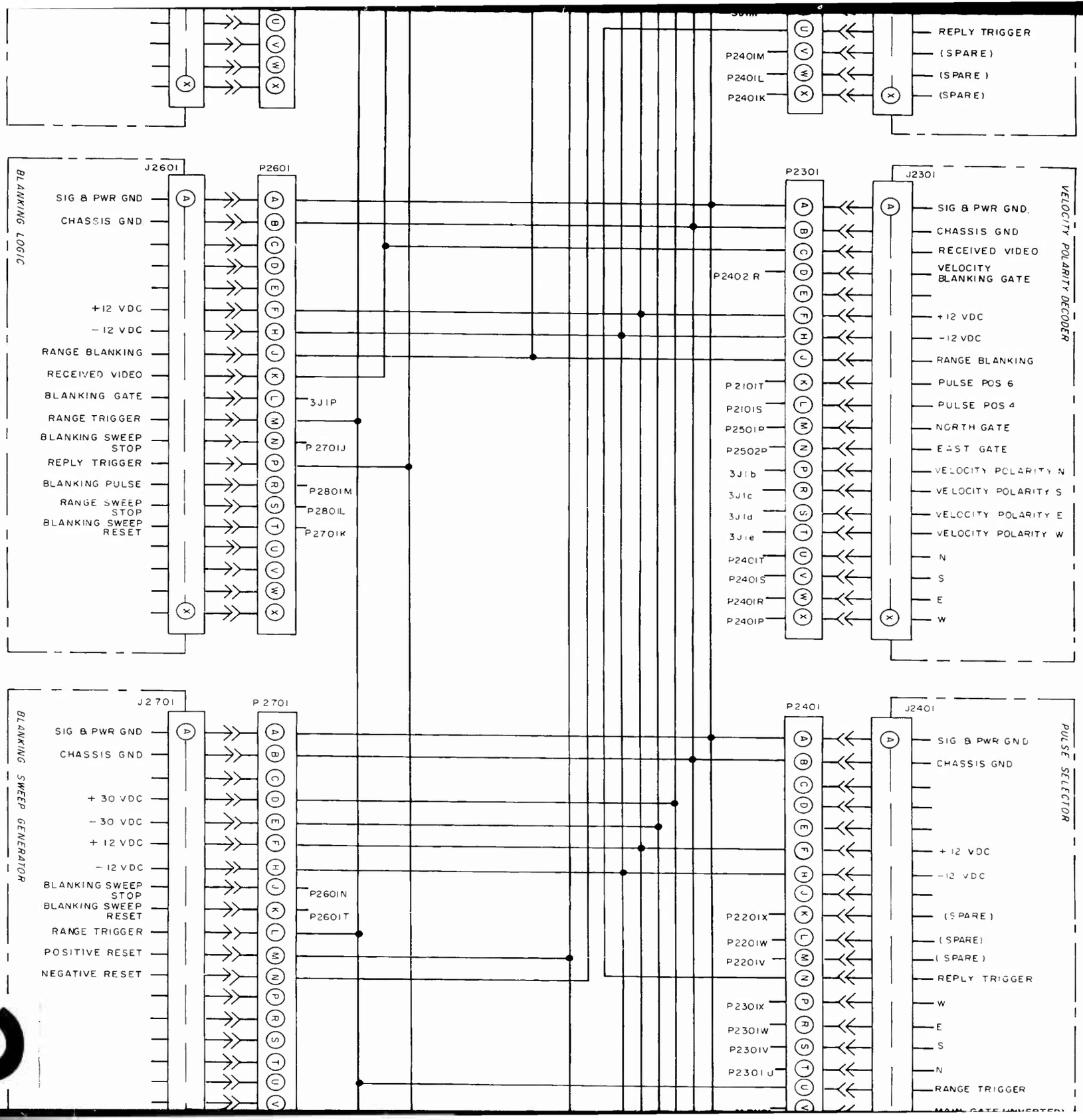


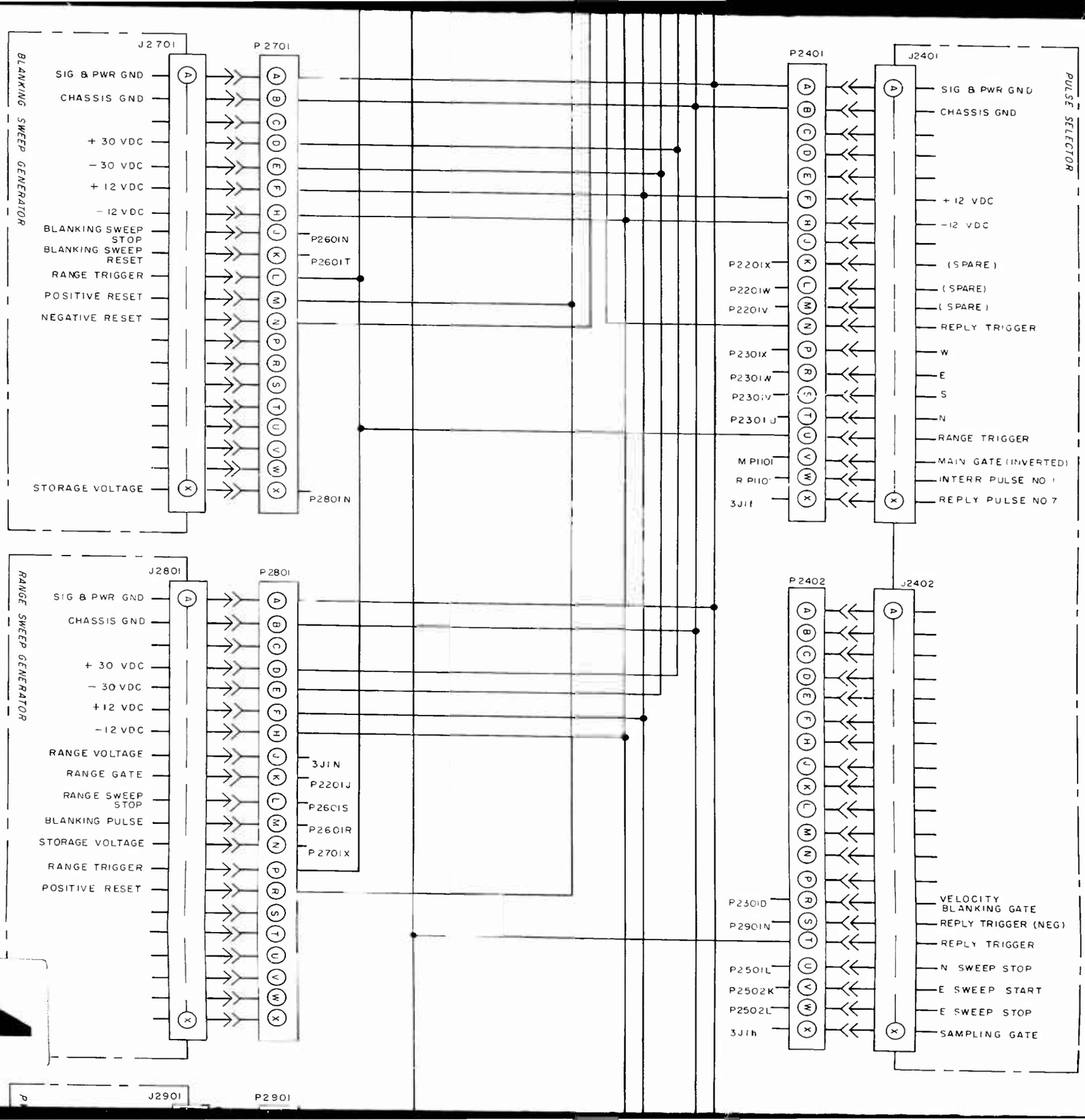
FIGURE 5-7.

INTERROGATOR ENCODER INTERCONNECTION DIAGRAM
(UNIT SERIES DESIGNATION 1000)


DELAY GENERATOR
J2101
SIG & PWR GND
CHASSIS GND
RECEIVED VIDEO
+30 VDC
-30 VDC
-12 VDC
PULSE POS -4
PULSE POS -6
PULSE POS -8
PULSE POS -10
PULSE POS -12
PULSE POS -20
P2101
P2301L
P2301K
P2201P
P2201N
P2201M
P2201L
THESE WIRES ARE TIED TO THEIR PROPER BUSSES INSIDE THE CHASSIS THE 3J1 TERMINATIONS ARE SHOWN ON EN — DECODER DIAGRAM
PWR & SIG GND
CHASSIC GND
+30 VDC
-30 VDC
+12 VDC
-12 VDC
N VELOCITY (POS) V TO P2501M
N VELOCITY (NEG) W TO P2501N
E VELOCITY (NEG) X TO P2502N
E VELOCITY (POS) Z TO P2502M
VELOCITY POLARITY N b TO P2301P
VELOCITY POLARITY S c TO P2301R
VELOCITY POLARITY E d TO P2301S
VELOCITY POLARITY W e TO P2301T
REPLY PULSE NO 7 f TO P2401X
REPLY TRIGGER g
SAMPLING GATE h TO P2402X
ABOVE-8 j TO P2201R
BELOW-10 k TO P2201S
CHANGING-12 m TO P2201T
RANGE VOLTAGE n TO P2801J
BLANKING GATE p TO P2601L
3J1
RECEIVED VIDEO J2001
TO N P1101
PWI OUTPUT J2004 TO P2901X
INDICATOR TRIGGER J2005 TO P2901R
P2402U
3J1V
3J1W
P2301M
P2501
P2502
J2501
SIG & PWR GND
CHASSIS GND
+30 VDC
-30 VDC
+12 VDC
-12 VDC
START SWEEP
STOP SWEEP
VELOCITY (POS)
VELOCITY (NEG)
GATE
NEGATIVE RESET
POSITIVE RESET
NORTH VELOCITY DECODER
J2201
P2201


STOP SWEEP
VELOCITY (POS)
VELOCITY (NEG)
GATE
NEGATIVE RESET
POSITIVE RESET
P2402U
3J1V
3J1W
P2301M
P2301L
P2301K
P2201P
P2201N
P2201M
P2201L
PULSE POS. – 4
PULSE POS –6
PULSE POS – 8
PULSE POS – 10
PULSE POS – 12
PULSE POS – 20
EAST VELOCITY DECODER
J2501
P2502
SIG & PWR GND
CHASSIS GND
+ 30 VDC
– 30 VDC
+ 12 VDC
– 12 VDC
START SWEEP
STOP SWEEP
VELOCITY (POS.)
VELOCITY (NEG)
GATE
NEGATIVE RESET
POSITIVE RESET
P2402V
P2402W
3J1Z
3J1X
P2301N
P2201
J2201
RELATIVE ALTITUDE (AND VELOCITY SCALE) DECODER
SIG & PWR GND
CHASSIS GND.
RECEIVED VIDEO
+ 12 VDC
– 12 VDC
RANGE GATE
RANGE BLANKING
PULSE POS – 20
PULSE POS – 12
PULSE POS – 10
PULSE POS – 8
ABOVE – 8
BELOW – 10
CHANGING – 12
REPLY TRIGGER
(SPARE)
(SPARE)
(SPARE)
P2801K
P2101X
P2101W
P2101V
P2101U
3J1j
3J1k
3J1m
P2401M
P2401L
P2401K
BLANKING LOGIC
J2601
P2601
SIG & PWR GND
CHASSIS GND
+12 VDC
– 12 VDC
RANGE BLANKING
RECEIVED VIDEO
BLANKING GATE
RANGE TRIGGER
BLANKING SWEEP
3J1P
P2301
J2301
VELOCITY POLARITY DECODER
SIG & PWR GND
CHASSIS GND
RECEIVED VIDEO
VELOCITY BLANKING GATE
+12 VDC
– 12 VDC
RANGE BLANKING
PULSE POS 6
PULSE POS 4
NORTH GATE
EAST GATE
P2402R
P2101T
P2101S
P2501P


BLANKING LOGIC
J2601
P2601
SIG & PWR GND
CHASSIS GND
+12 VDC
-12 VDC
RANGE BLANKING
RECEIVED VIDEO
BLANKING GATE
RANGE TRIGGER
BLANKING SWEEP STOP
REPLY TRIGGER
BLANKING PULSE
RANGE SWEEP STOP
BLANKING SWEEP RESET
3J1P
P2701J
P2801M
P2801L
P2701K
P2401M
P2401L
P2401K
REPLY TRIGGER
(SPARE)
(SPARE)
(SPARE)
P2301
J2301
VELOCITY POLARITY DECODER
P2402 R
P2101T
P2101S
P2501P
P2502P
3J1b
3J1c
3J1d
3J1e
P2401T
P2401S
P2401R
P2401P
SIG & PWR GND
CHASSIS GND
RECEIVED VIDEO
VELOCITY BLANKING GATE
+12 VDC
-12 VDC
RANGE BLANKING
PULSE POS 6
PULSE POS 4
NORTH GATE
EAST GATE
VELOCITY POLARITY N
VELOCITY POLARITY S
VELOCITY POLARITY E
VELOCITY POLARITY W
N
S
E
W
BLANKING SWEEP GENERATOR
J2701
P2701
SIG & PWR GND
CHASSIS GND
+30 VDC
-30 VDC
+12 VDC
-12 VDC
BLANKING SWEEP STOP
BLANKING SWEEP RESET
RANGE TRIGGER
POSITIVE RESET
NEGATIVE RESET
P2601N
P2601T
P2401
J2401
PULSE SELECTOR
P2201X
P2201W
P2201V
P2301X
P2301W
P2301V
P2301U
SIG & PWR GND
CHASSIS GND
+12 VDC
-12 VDC
(SPARE)
(SPARE)
(SPARE)
REPLY TRIGGER
W
E
S
N
RANGE TRIGGER


BLANKING SWEEP GENERATOR
J2701
P2701
SIG & PWR GND
CHASSIS GND
+ 30 VDC
− 30 VDC
+ 12 VDC
− 12 VDC
BLANKING SWEEP STOP
BLANKING SWEEP RESET
RANGE TRIGGER
POSITIVE RESET
NEGATIVE RESET
STORAGE VOLTAGE
P2601N
P2601T
P2801N
RANGE SWEEP GENERATOR
J2801
P2801
SIG & PWR GND
CHASSIS GND
+ 30 VDC
− 30 VDC
+12 VDC
−12 VDC
RANGE VOLTAGE
RANGE GATE
RANGE SWEEP STOP
BLANKING PULSE
STORAGE VOLTAGE
RANGE TRIGGER
POSITIVE RESET
3J1N
P2201J
P2601S
P2601R
P2701X
J2901
P2901
P2401
J2401
PULSE SELECTOR
SIG & PWR GND
CHASSIS GND
+ 12 VDC
−12 VDC
(SPARE)
(SPARE)
(SPARE)
REPLY TRIGGER
W
E
S
N
RANGE TRIGGER
MAIN GATE (INVERTED)
INTERR PULSE NO 1
REPLY PULSE NO 7
P2201X
P2201W
P2201V
P2301X
P2301W
P2301V
P2301J
M P1101
R P110'
3J1f
P2402
J2402
VELOCITY BLANKING GATE
REPLY TRIGGER (NEG)
REPLY TRIGGER
N SWEEP STOP
E SWEEP START
E SWEEP STOP
SAMPLING GATE
P2301D
P2901N
P2501L
P2502K
P2502L
3J1h

4

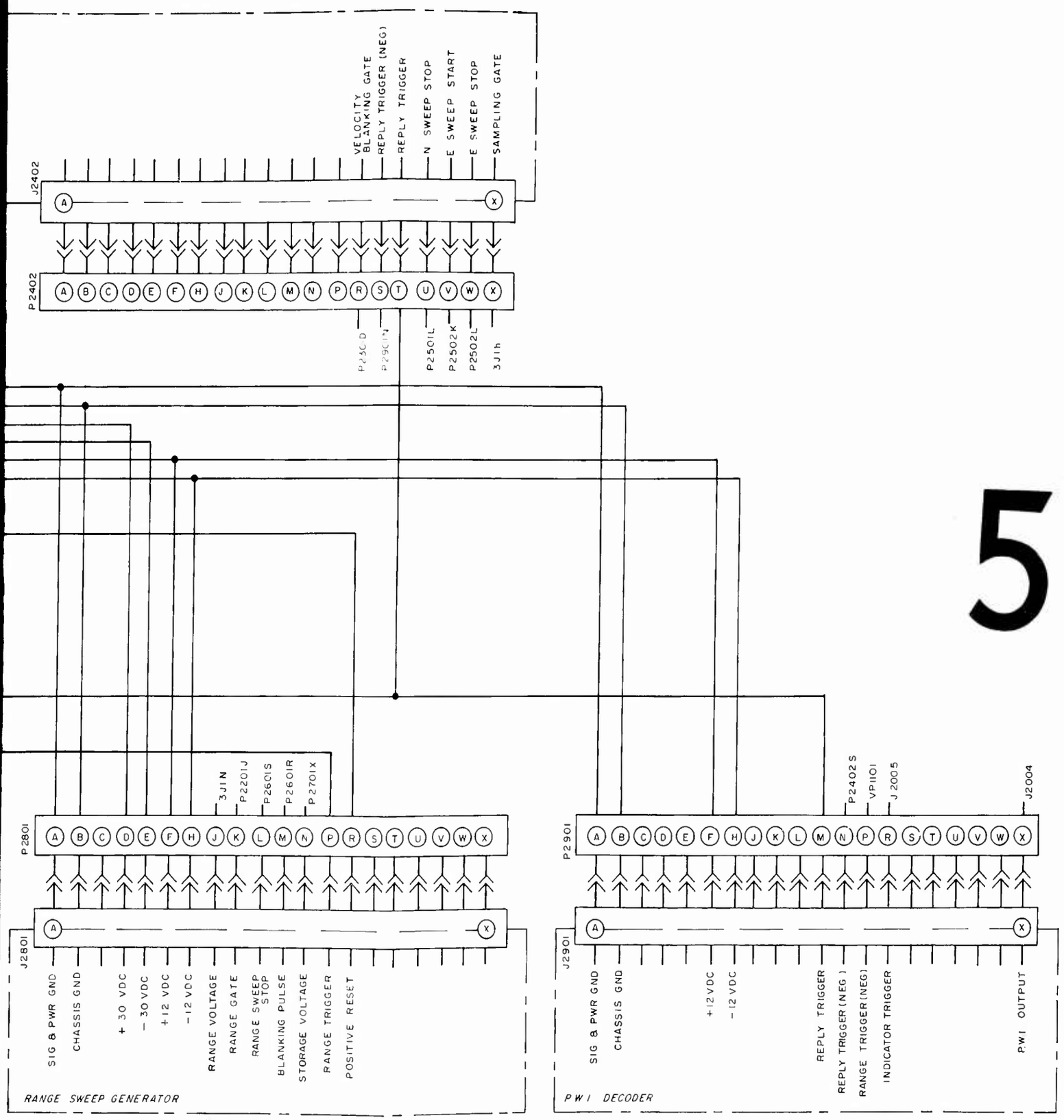
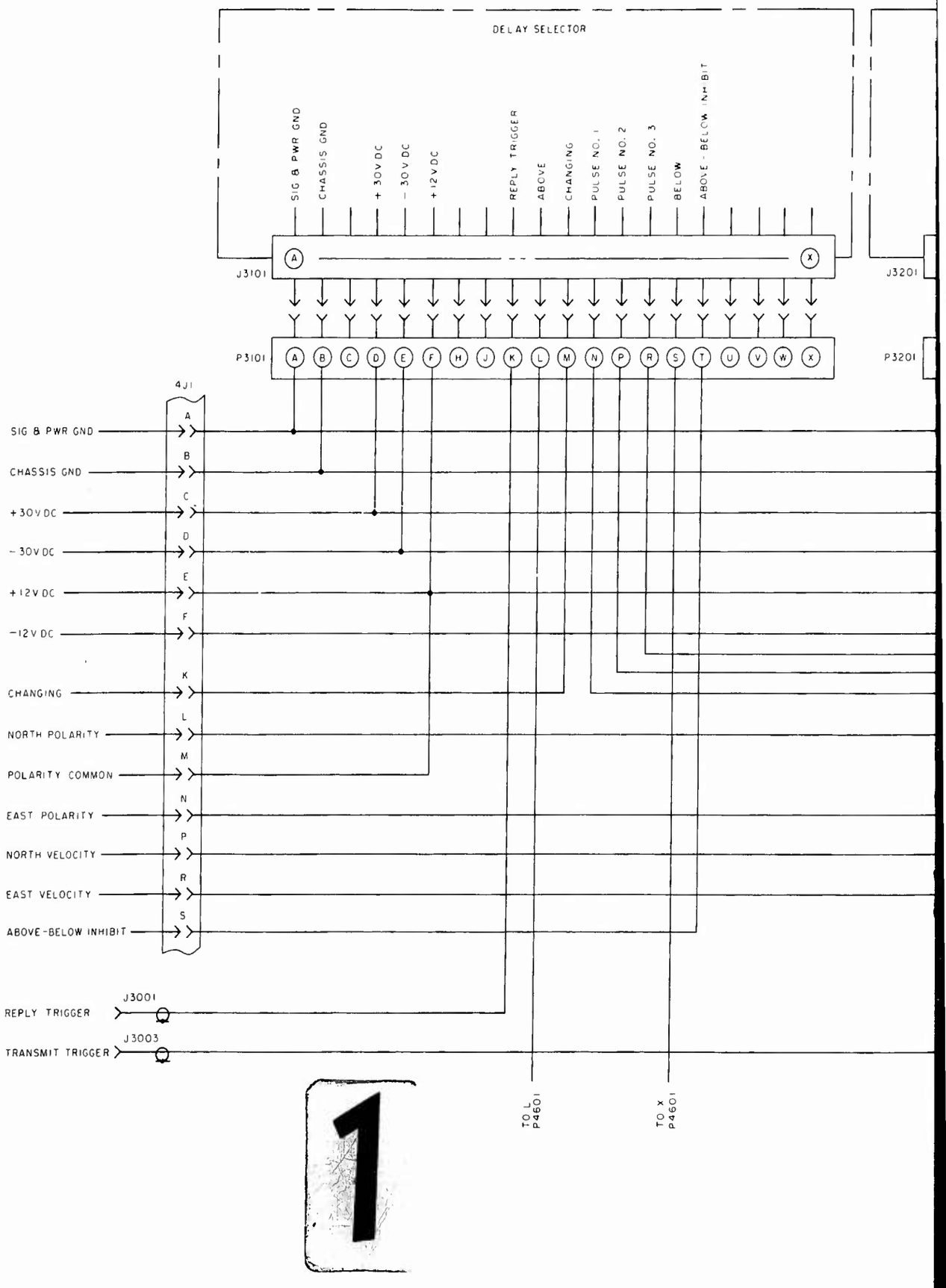
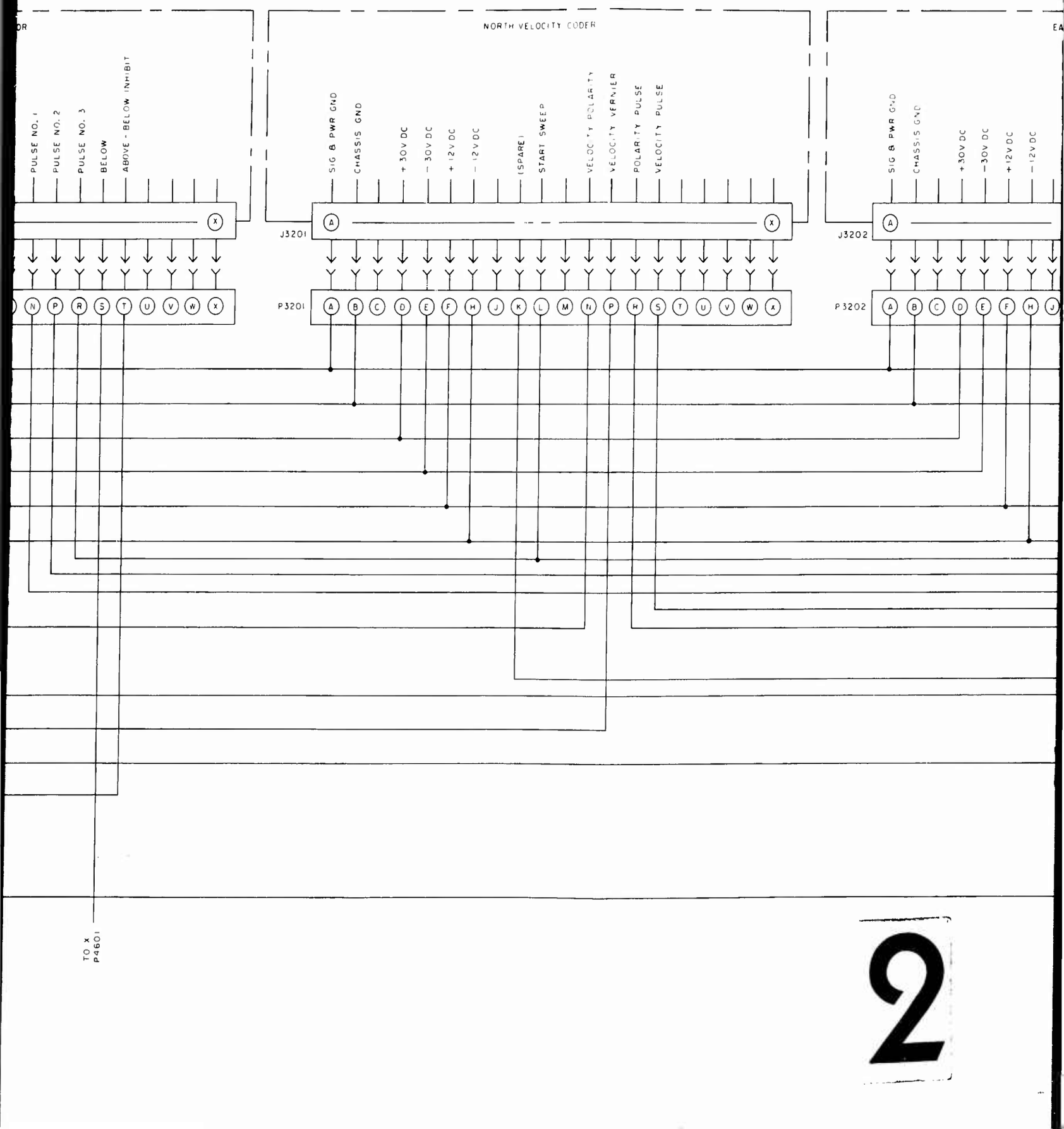


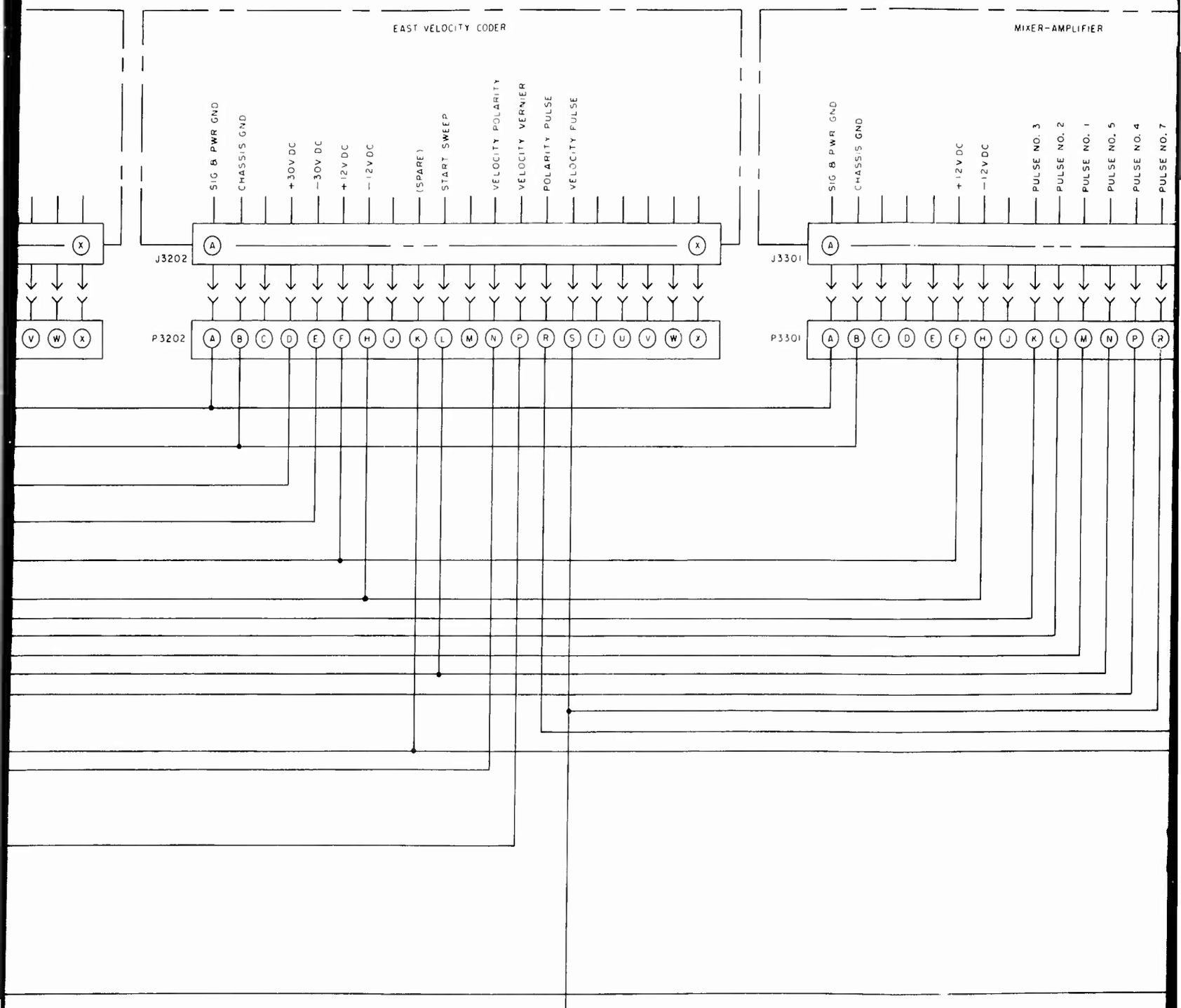
FIGURE 5-8

INTERROGATOR DECODER INTERCONNECTION DIAGRAM
(UNIT SERIES DESIGNATION 2000)


DELAY SELECTOR
SIG & PWR GND
CHASSIS GND
+30V DC
-30V DC
+12V DC
REPLY TRIGGER
ABOVE
CHANGING
PULSE NO. 1
PULSE NO. 2
PULSE NO. 3
BELOW
ABOVE - BELOW INH BIT
J3101
J3201
P3101
P3201
4J1
SIG & PWR GND
CHASSIS GND
+30V DC
-30V DC
+12V DC
-12V DC
CHANGING
NORTH POLARITY
POLARITY COMMON
EAST POLARITY
NORTH VELOCITY
EAST VELOCITY
ABOVE-BELOW INHIBIT
REPLY TRIGGER
J3001
TRANSMIT TRIGGER
J3003
TO L P4601
TO X P4601
1


NORTH VELOCITY CODER
PULSE NO. 1
PULSE NO. 2
PULSE NO. 3
BELOW
ABOVE - BELOW INHIBIT
SIG & PWR GND
CHASSIS GND
+ 30V DC
- 30V DC
+ 12V DC
- 12V DC
(SPARE)
START SWEEP
VELOCITY POLARITY
VELOCITY VERNIER
POLARITY PULSE
VELOCITY PULSE
J3201
P3201
J3202
P3202
TO x
P4601

2



3

TRANSPONDER ENCOD
(UNIT SERI

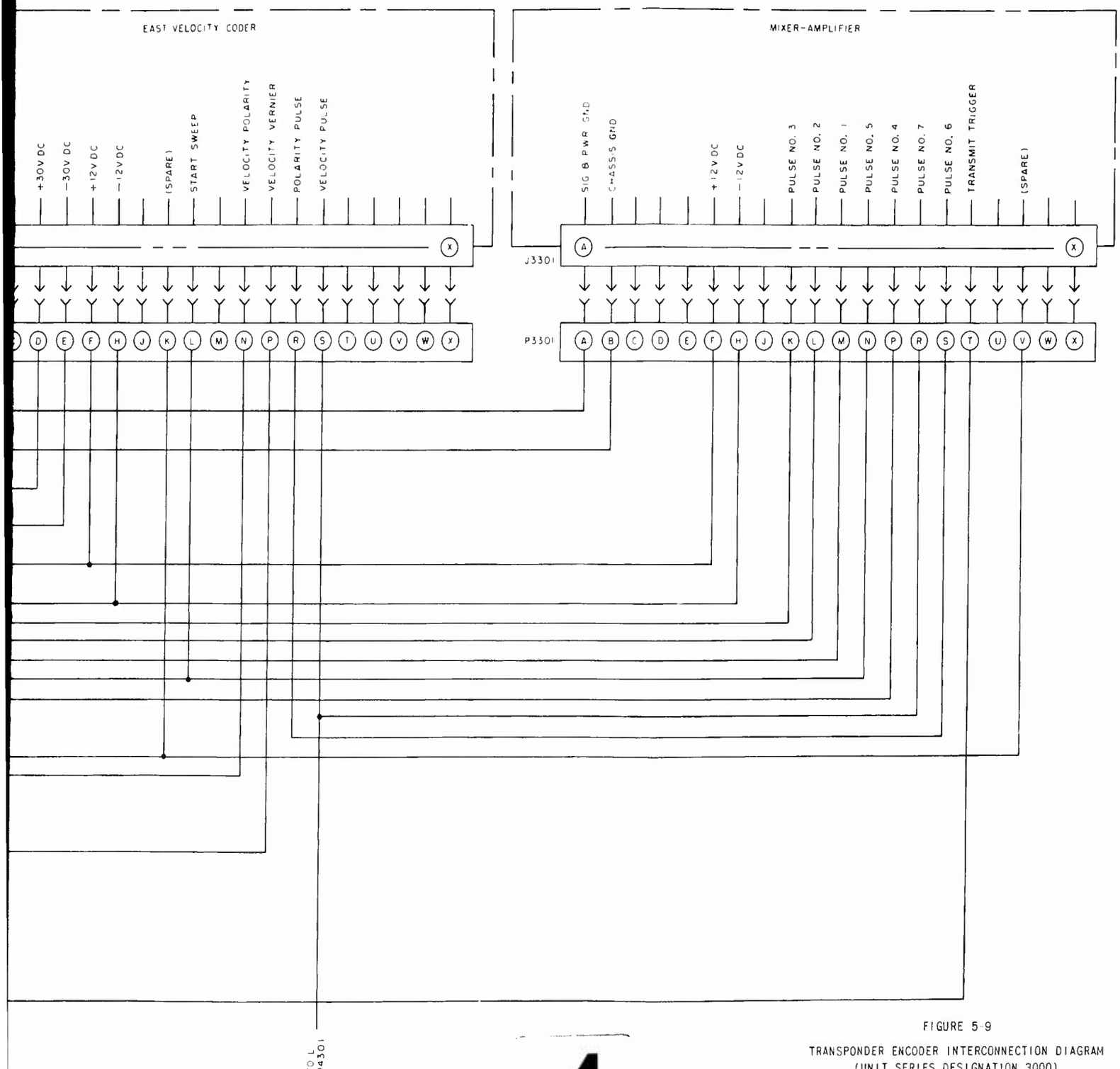
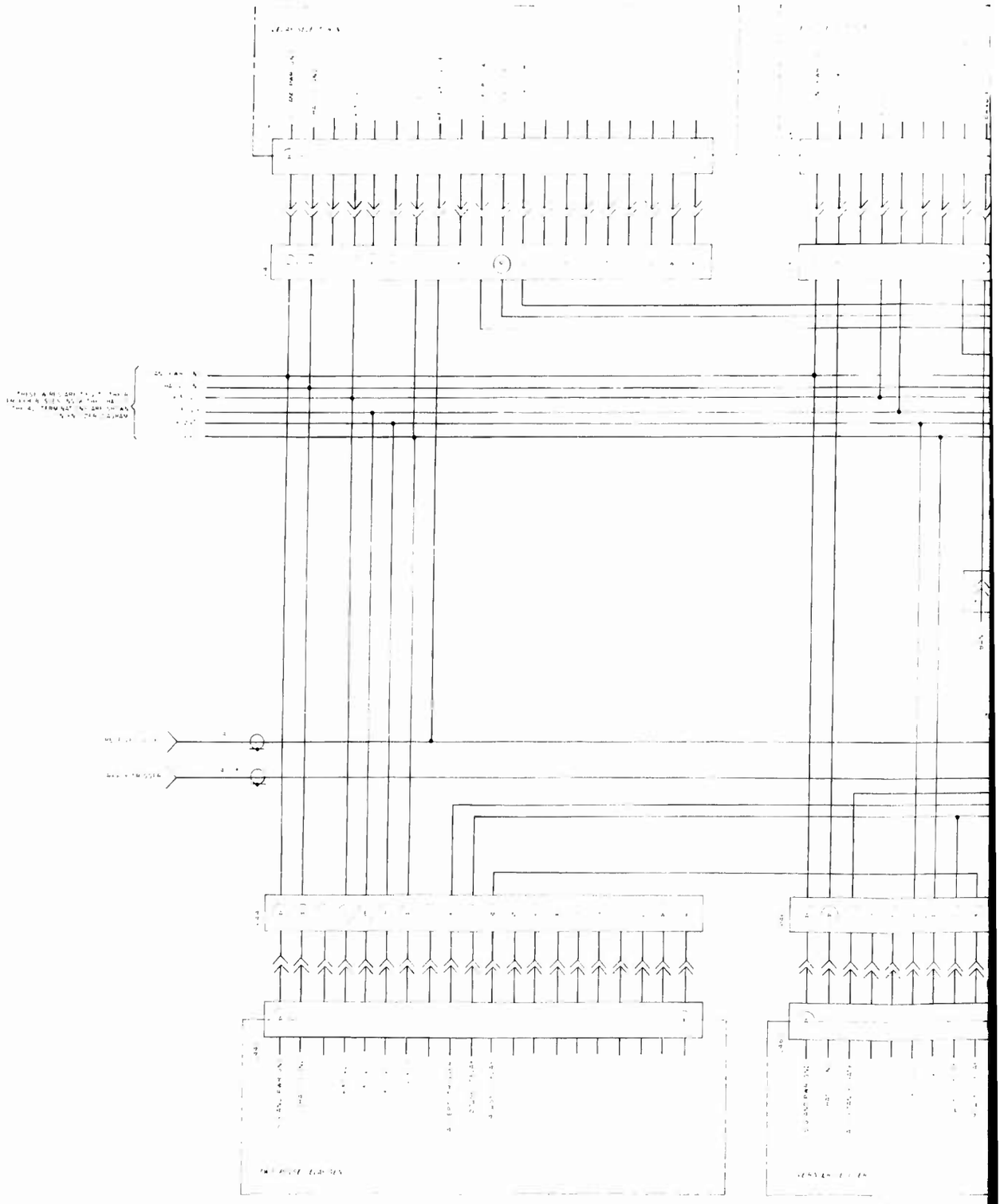
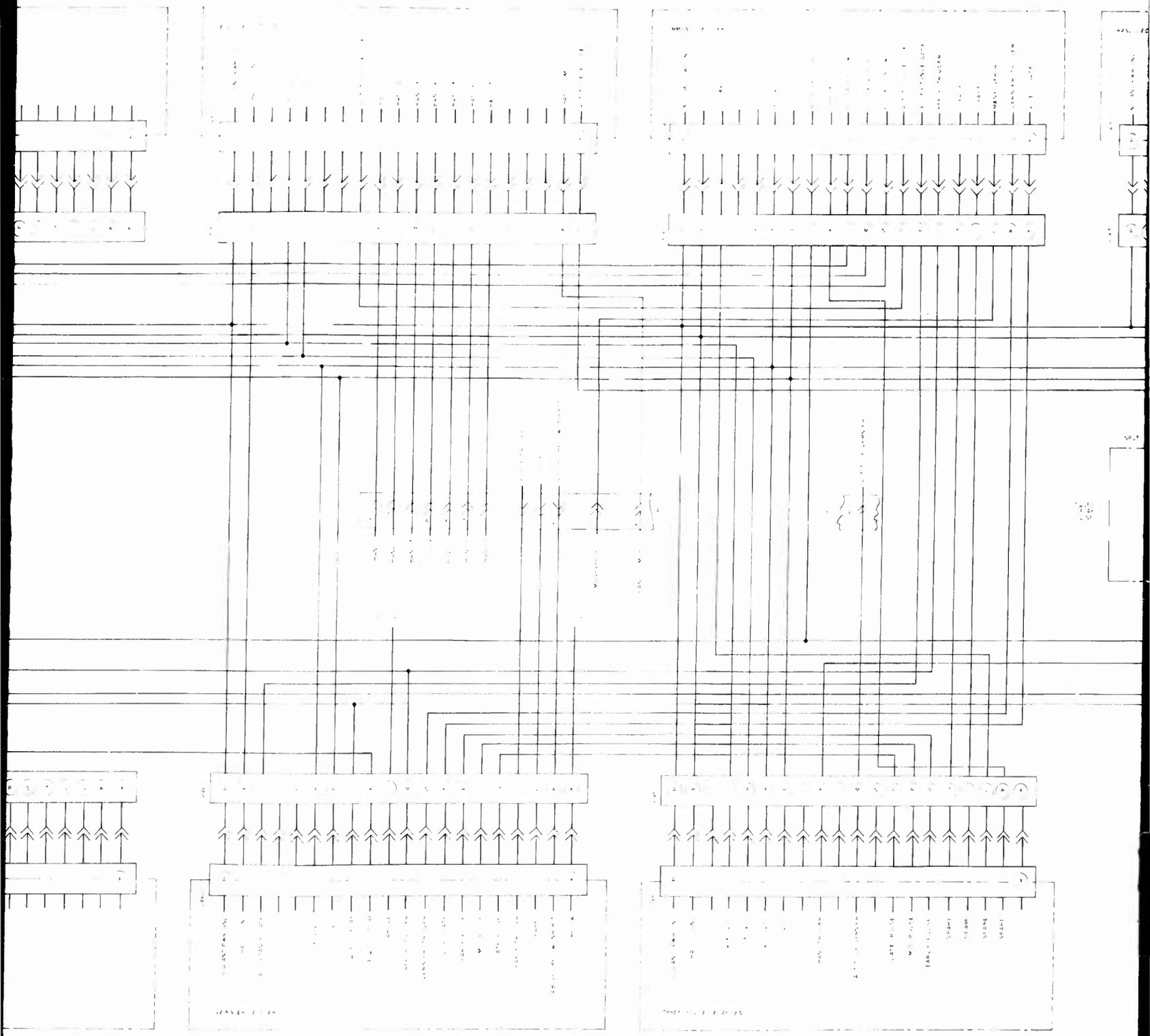


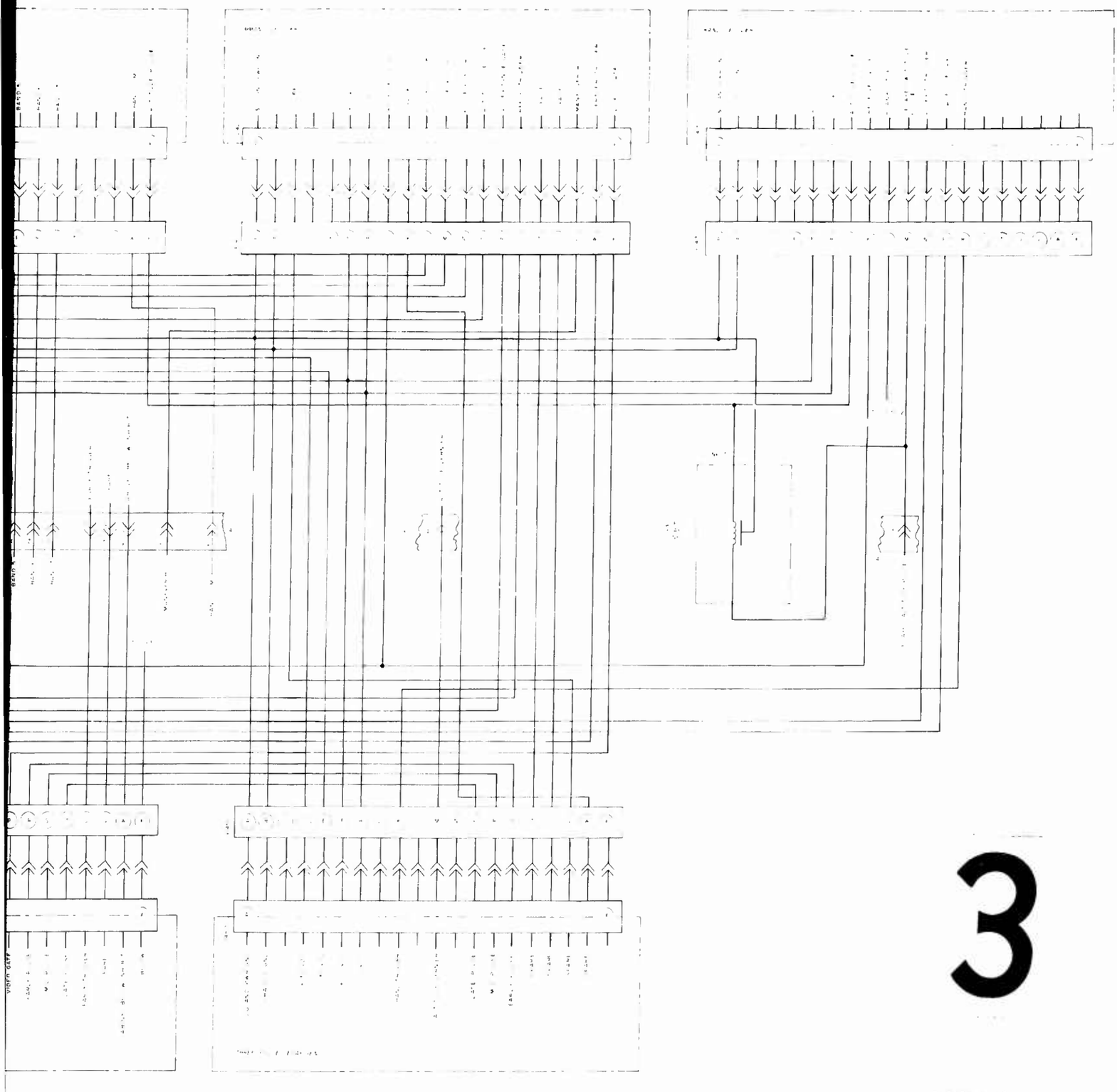
FIGURE 5-9

TRANSPONDER ENCODER INTERCONNECTION DIAGRAM
(UNIT SERIES DESIGNATION 3000)



1

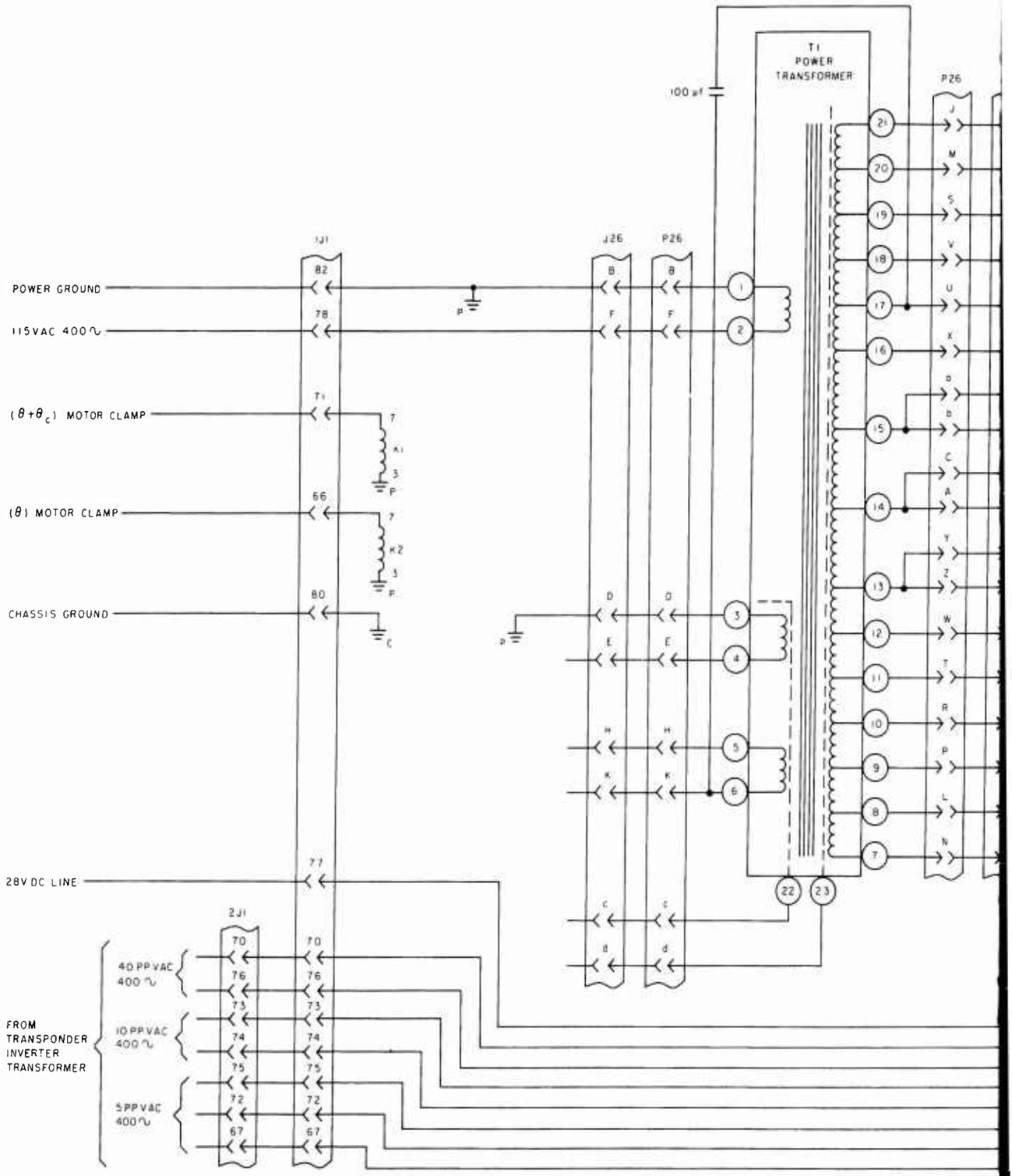


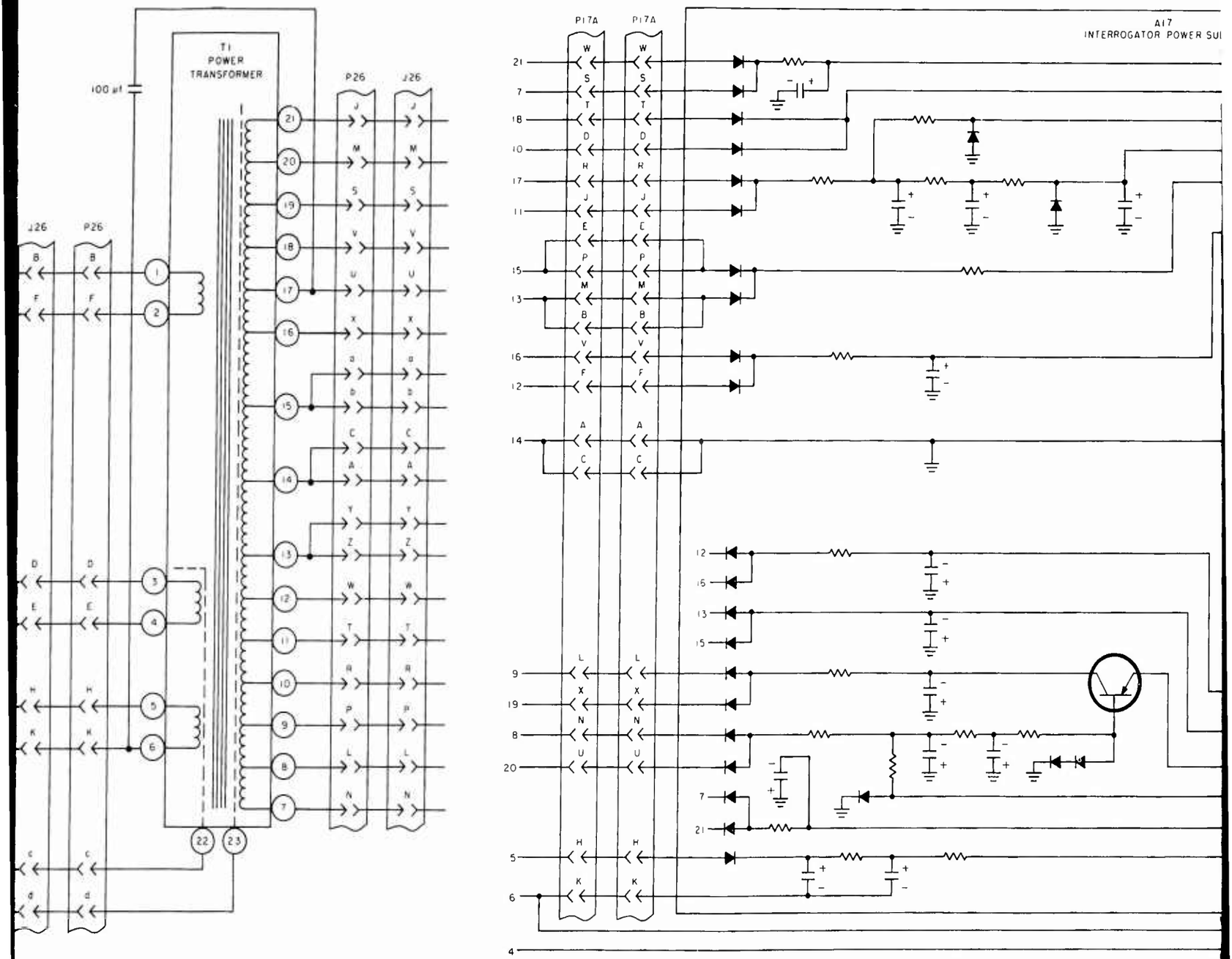


3

FIGURE 5-10.

TRANSPONDER DECODER INTERCONNECTION DIAGRAM
(UNIT SERIES DESIGNATION 4000)


T1
POWER
TRANSFORMER
100 μf
1J1
J26
P26
P26
POWER GROUND
115VAC 400∿
(θ+θc) MOTOR CLAMP
(θ) MOTOR CLAMP
CHASSIS GROUND
28V DC LINE
2J1
FROM
TRANSPONDER
INVERTER
TRANSFORMER
40 PP VAC
400 ∿
10 PP VAC
400 ∿
5PP VAC
400∿


T1
POWER
TRANSFORMER
100 µf
J26
P26
P17A
P17A
A17
INTERROGATOR POWER SUI

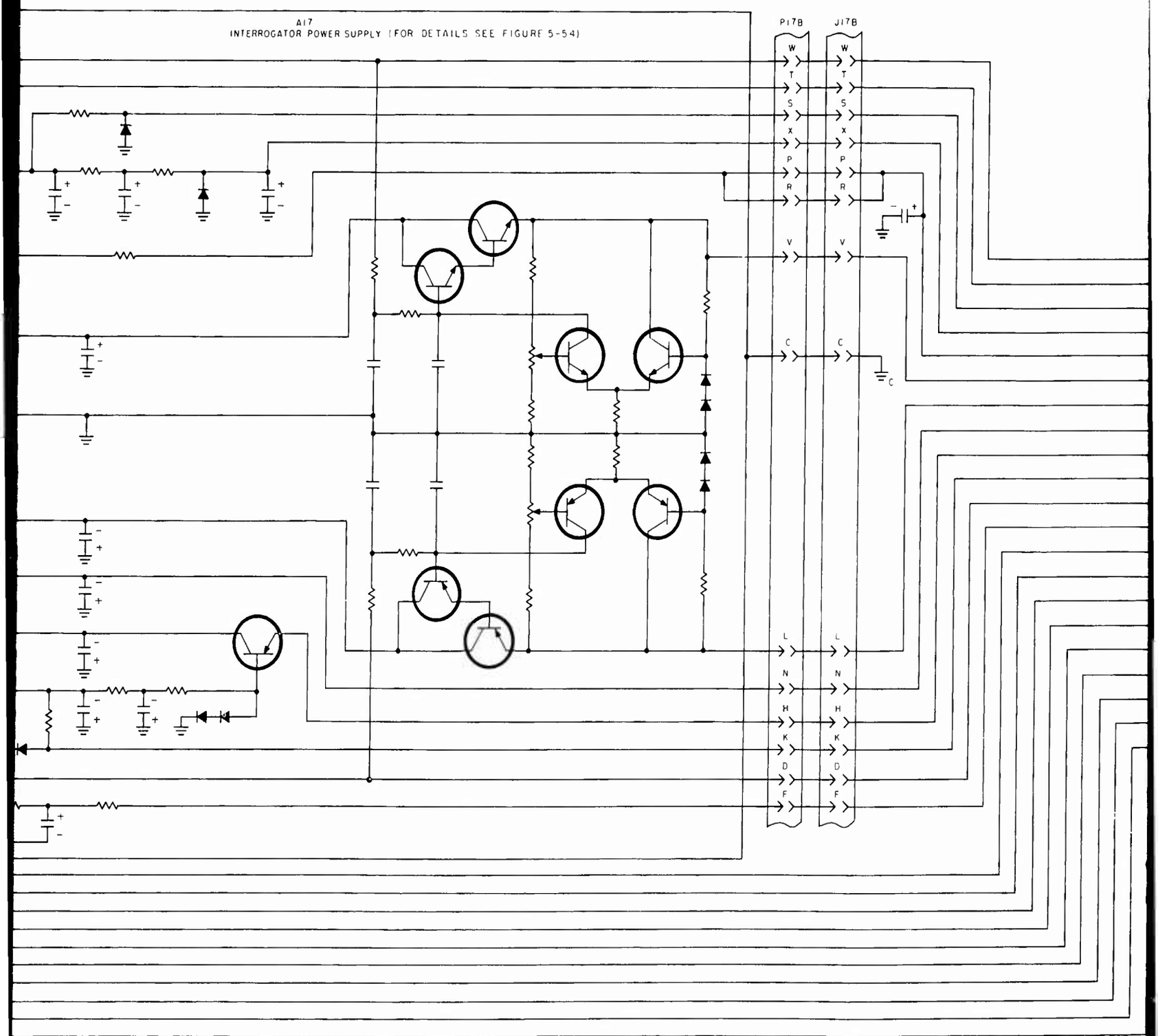


FIGURE 5-1

INTERROGATOR COMPUTER POWER SC

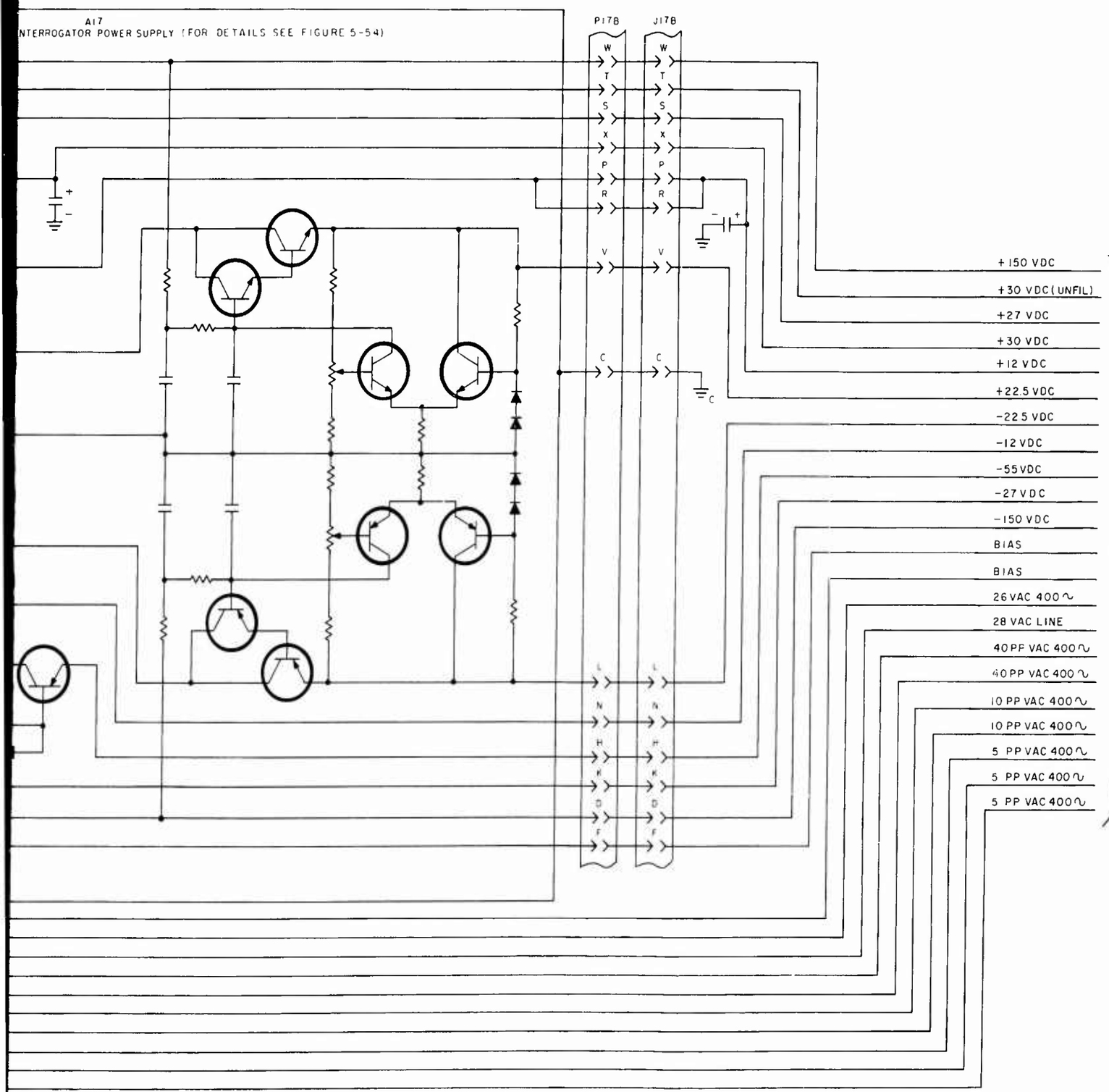
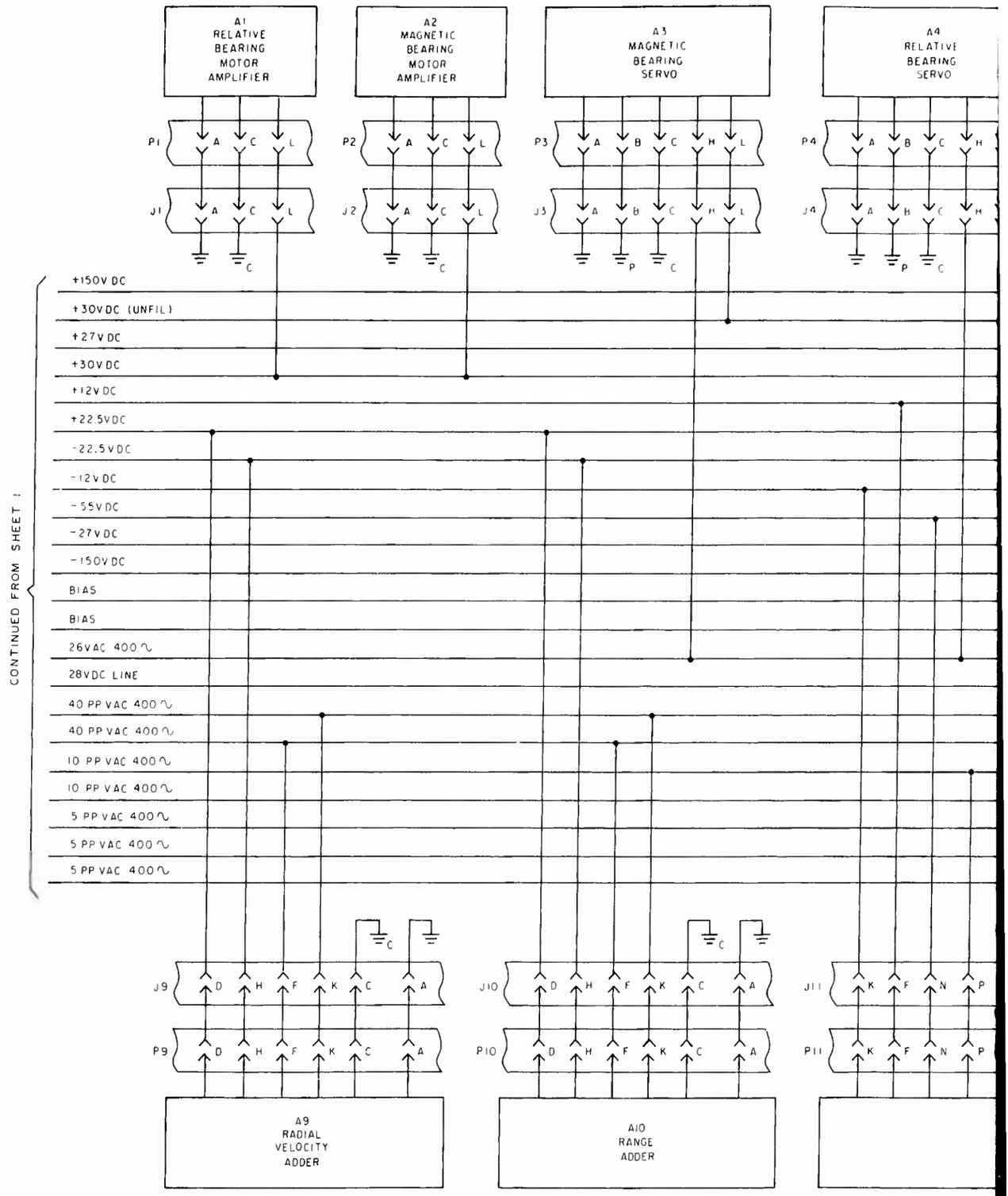


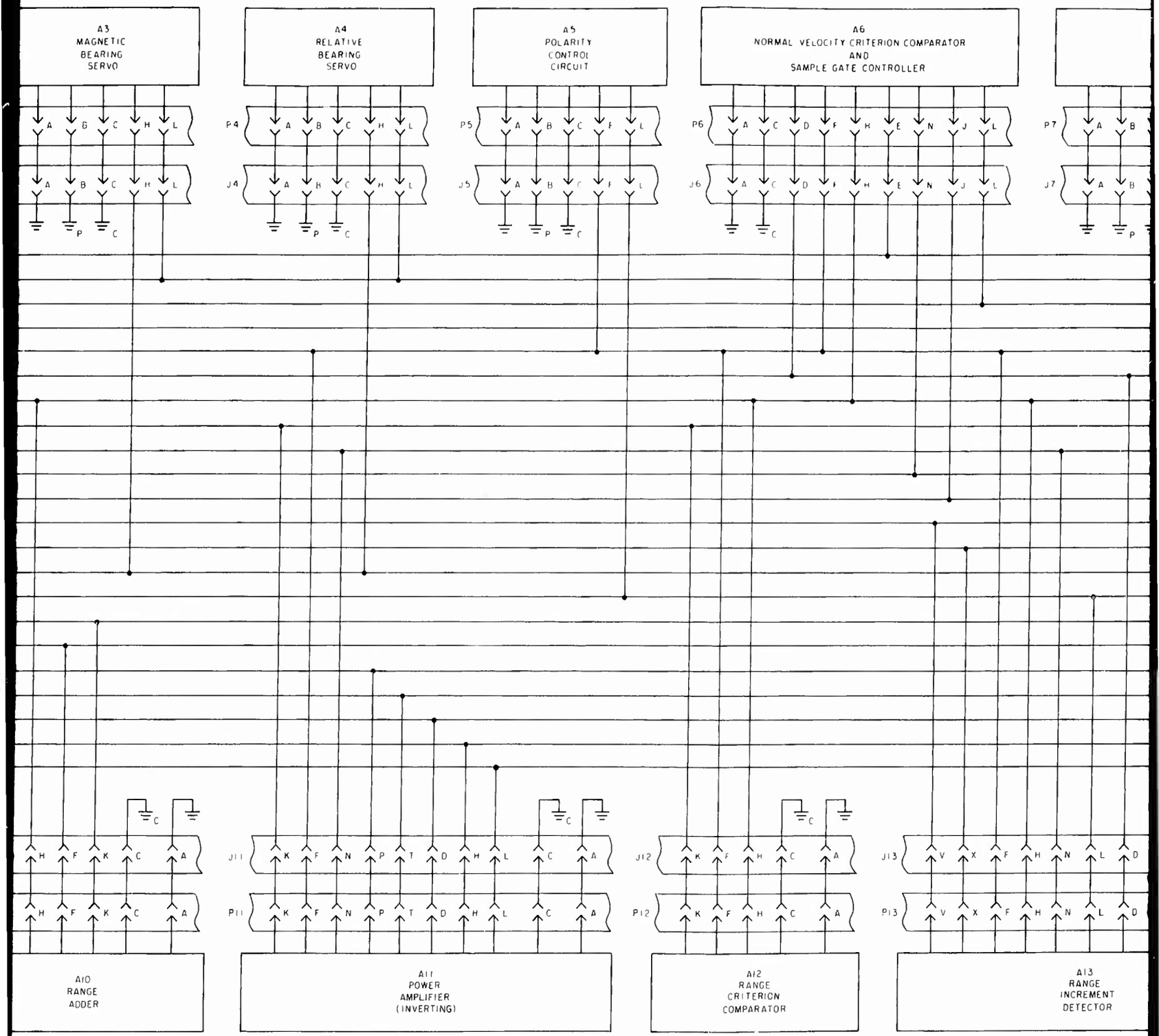
FIGURE 5-11.

INTERROGATOR COMPUTER POWER SCHEMATIC (SHEET 1 OF 2)

4


A1 RELATIVE BEARING MOTOR AMPLIFIER
A2 MAGNETIC BEARING MOTOR AMPLIFIER
A3 MAGNETIC BEARING SERVO
A4 RELATIVE BEARING SERVO
P1
J1
P2
J2
P3
J3
P4
J4
CONTINUED FROM SHEET 1
+150V DC
+30VDC (UNFIL)
+27V DC
+30V DC
+12V DC
+22.5VDC
-22.5VDC
-12V DC
-55V DC
-27V DC
-150V DC
BIAS
BIAS
26VAC 400∿
28VDC LINE
40 PP VAC 400∿
40 PP VAC 400∿
10 PP VAC 400∿
10 PP VAC 400∿
5 PP VAC 400∿
5 PP VAC 400∿
5 PP VAC 400∿
J9
P9
J10
P10
J11
P11
A9 RADIAL VELOCITY ADDER
A10 RANGE ADDER

1


A3
MAGNETIC
BEARING
SERVO
A4
RELATIVE
BEARING
SERVO
A5
POLARITY
CONTROL
CIRCUIT
A6
NORMAL VELOCITY CRITERION COMPARATOR
AND
SAMPLE GATE CONTROLLER
P4
J4
P5
J5
P6
J6
P7
J7
A10
RANGE
ADDER
A11
POWER
AMPLIFIER
(INVERTING)
A12
RANGE
CRITERION
COMPARATOR
A13
RANGE
INCREMENT
DETECTOR
P11
J11
P12
J12
P13
J13

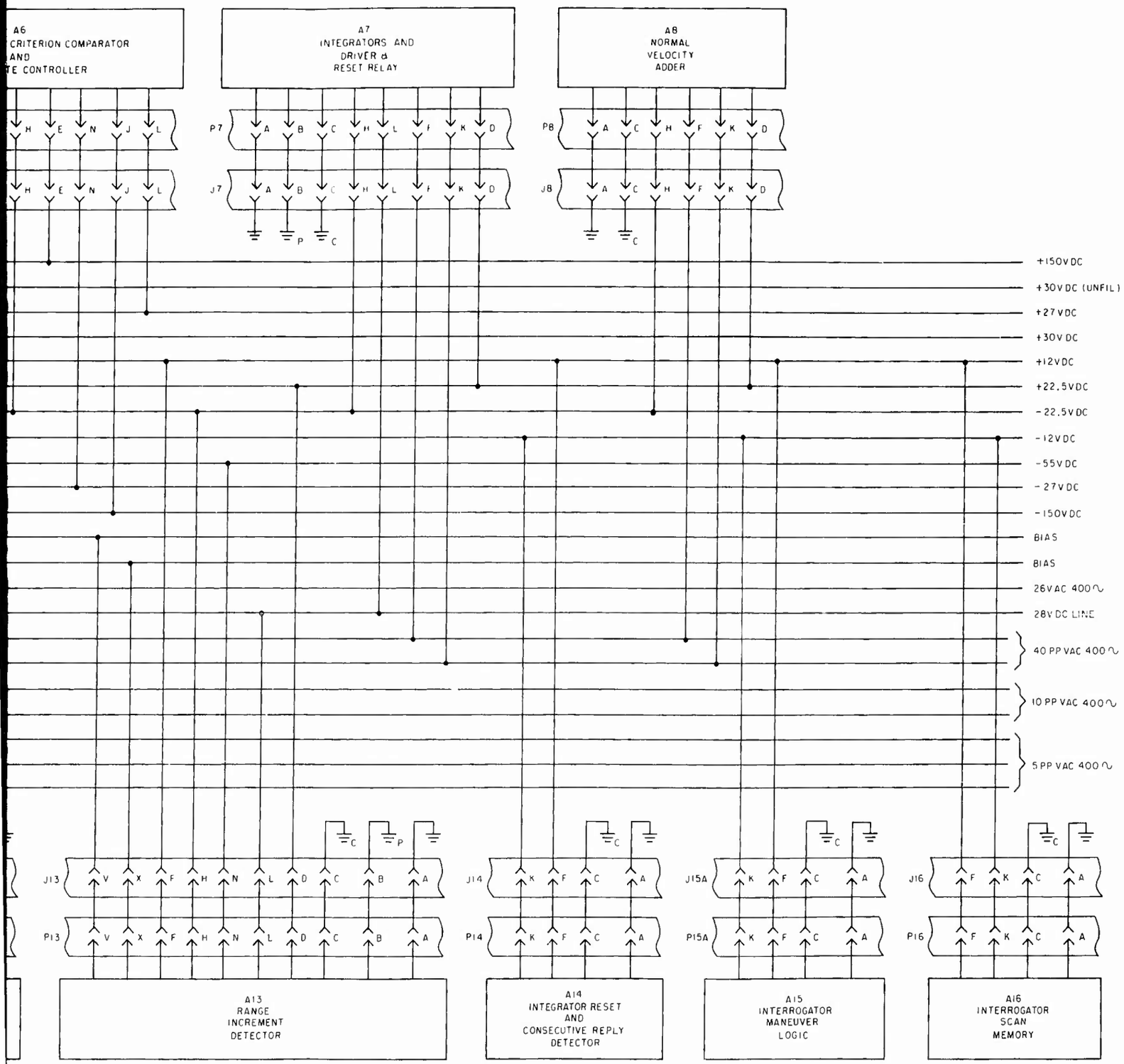


FIGURE 5-11.

INTERROGATOR COMPUTER POWER SCHEMATIC (SHEET 2 OF 2)

3

CORE - E I - 12 STACK 1.0"
SECONDARY BIFILAR WOUND
ALL WINDINGS NO 26 SWG

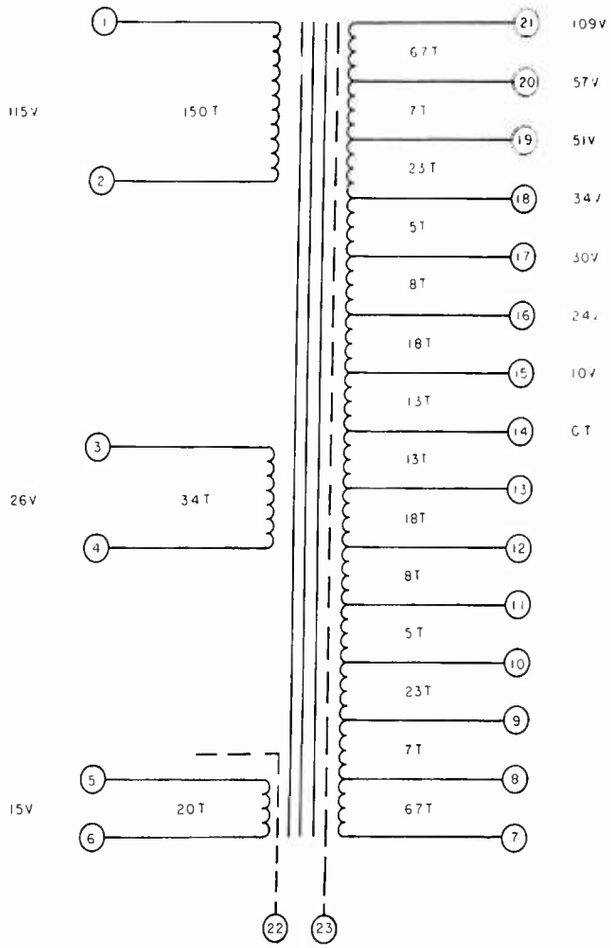
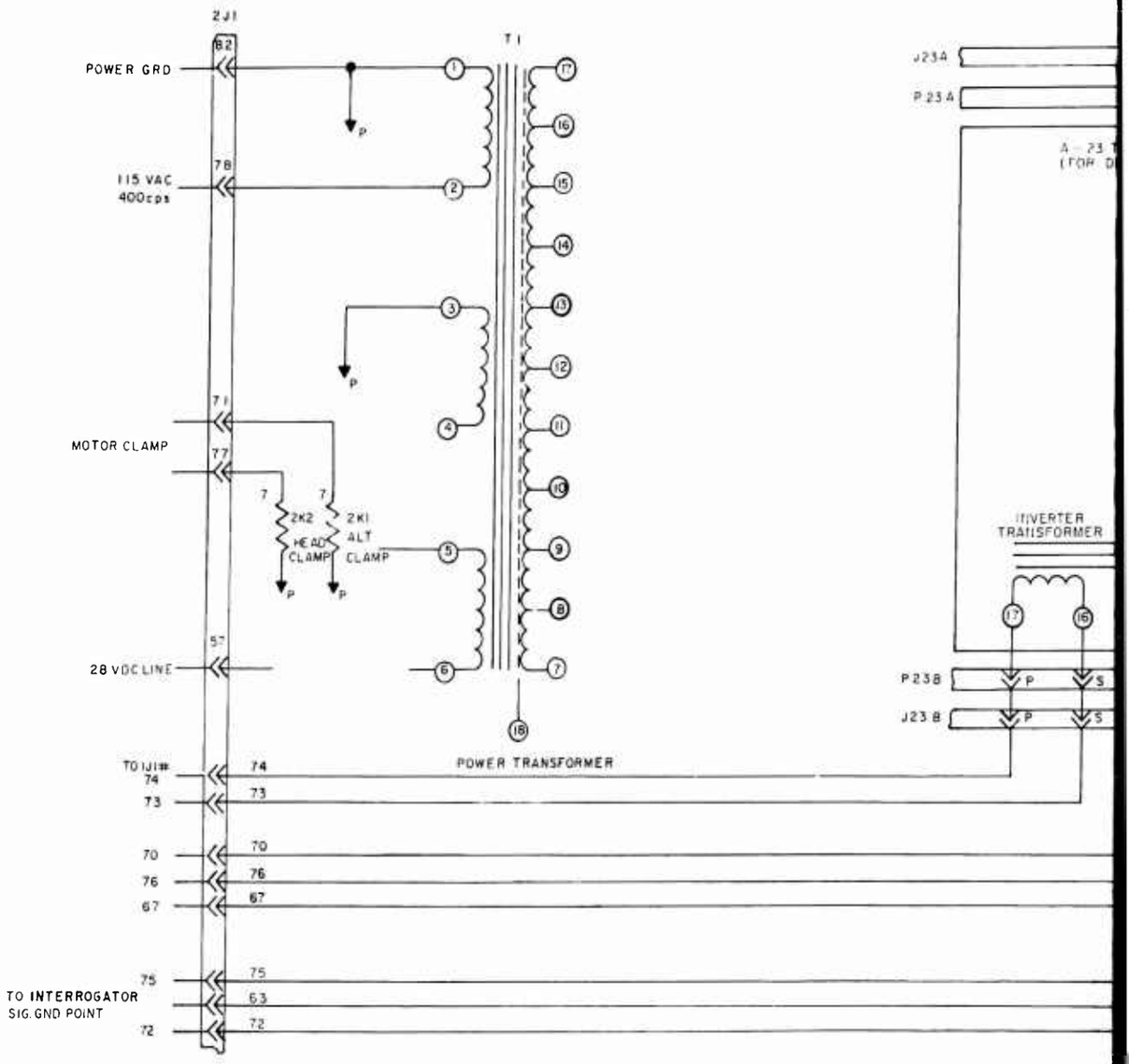
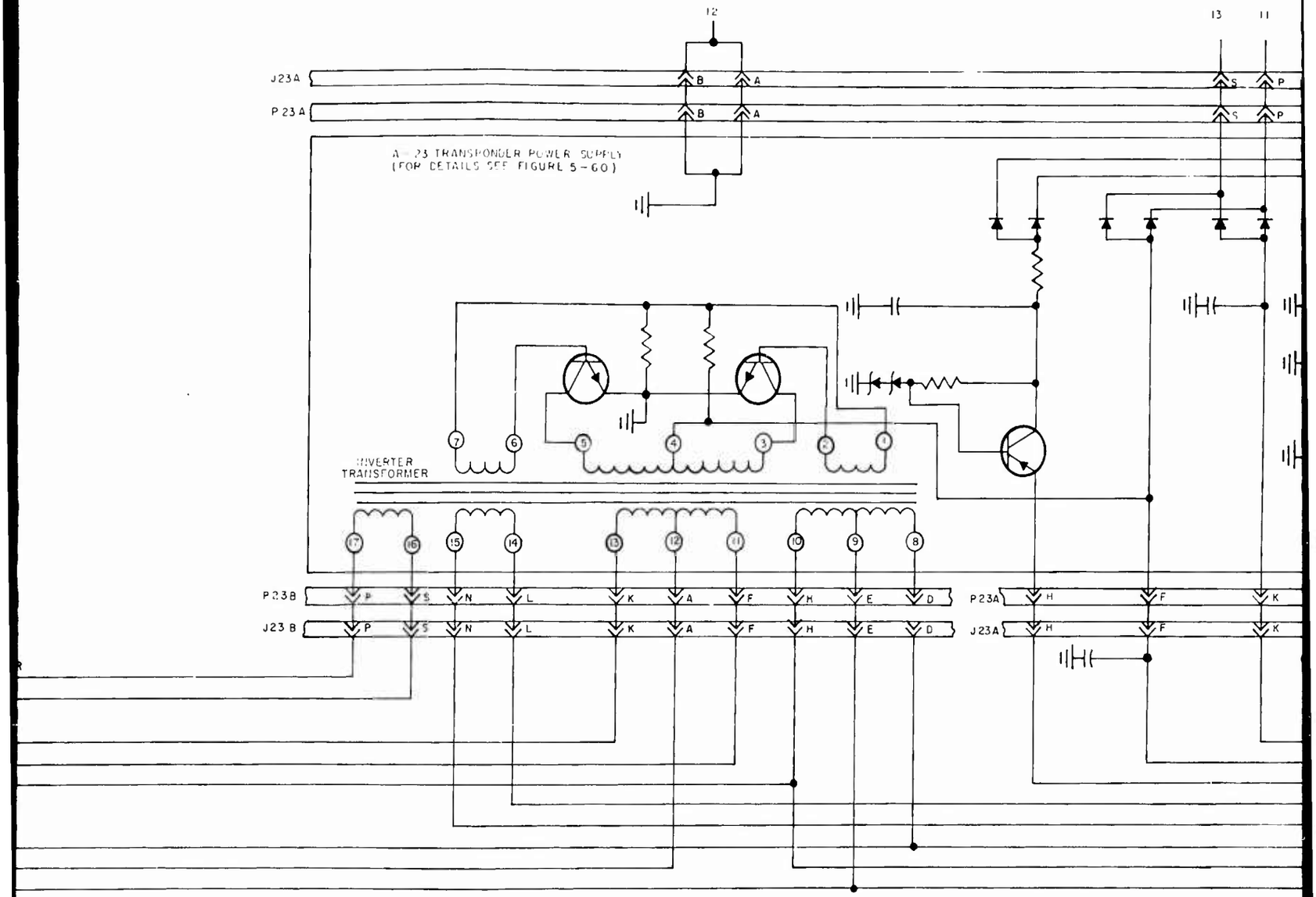
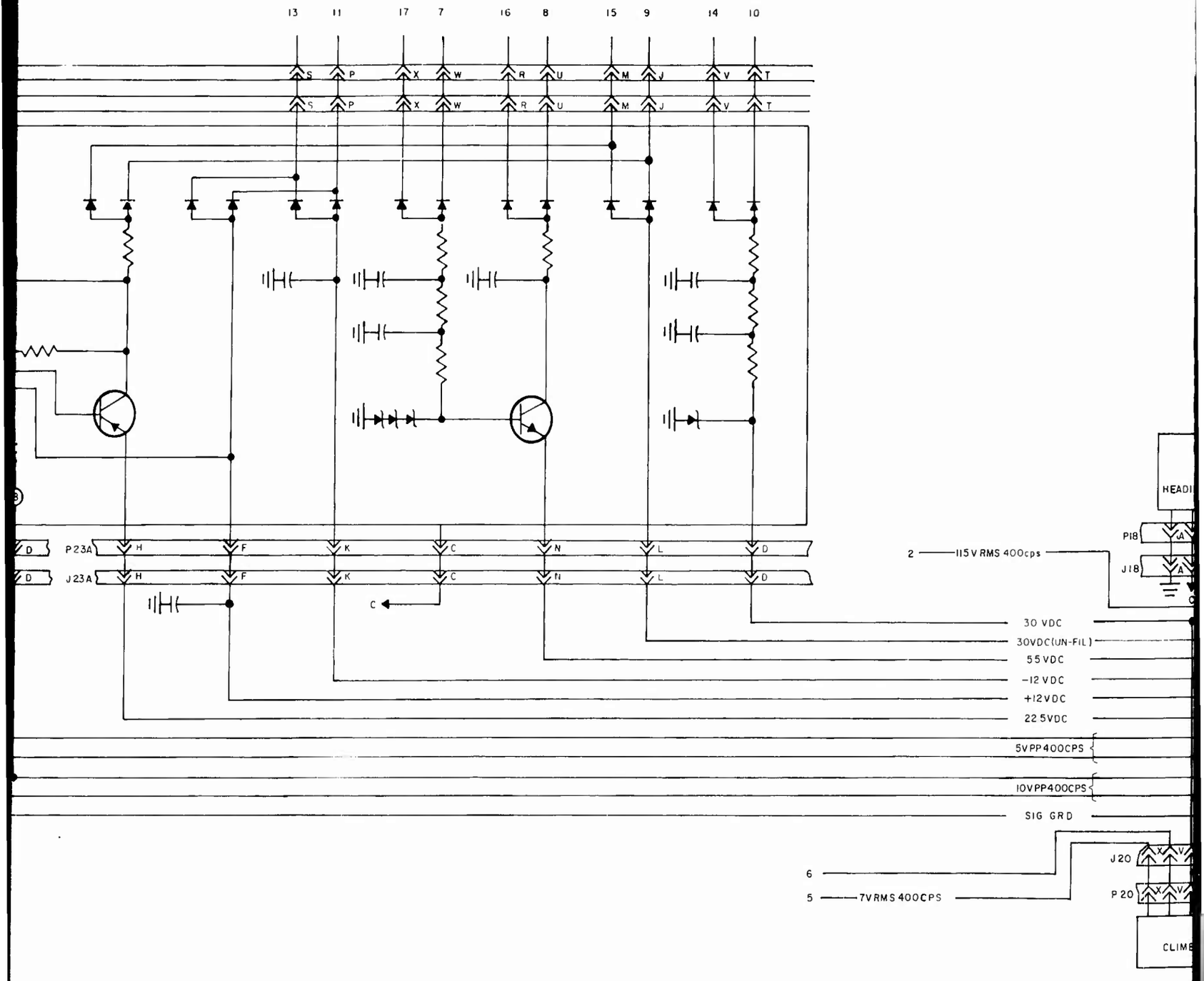


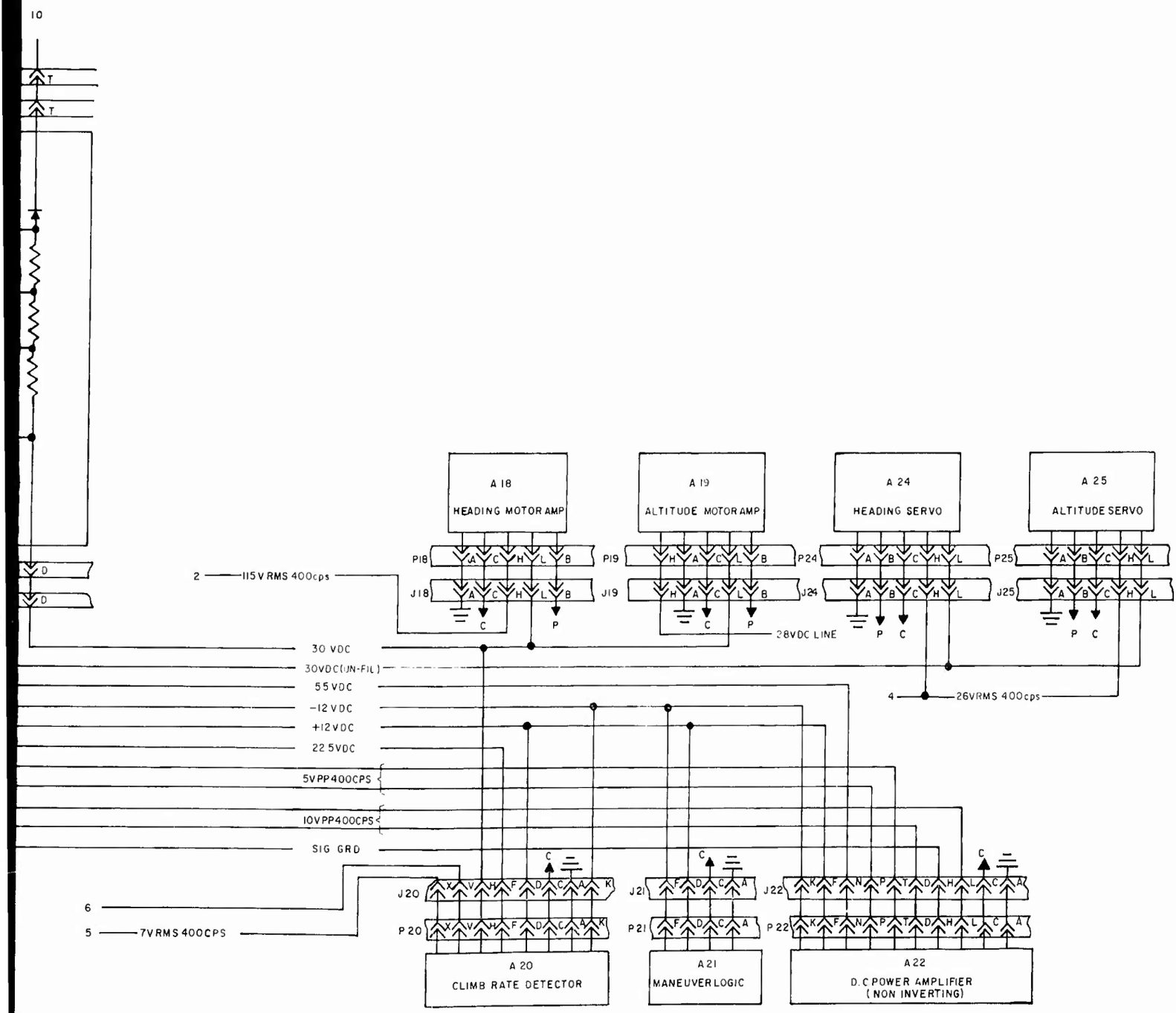
FIGURE 5-12. INTERROGATOR POWER TRANSFORMER


2J1
T1
POWER GRD
82
115 VAC
400cps
78
MOTOR CLAMP
71
77
2K2
HEAD
CLAMP
2K1
ALT
CLAMP
28 VDC LINE
57
TO 1J1#
74
73
70
76
67
75
TO INTERROGATOR
SIG.GND POINT
63
72
POWER TRANSFORMER
J234
P234
INVERTER
TRANSFORMER
P238
J238
P
S

1


J23A
P23A
A-23 TRANSPONDER POWER SUPPLY
(FOR DETAILS SEE FIGURE 5-60)
INVERTER
TRANSFORMER
P23B
J23B
P23A
J23A


13
11
17
7
16
8
15
9
14
10
S
P
X
W
R
U
M
J
V
T
P23A
J23A
H
F
K
C
N
L
D
2
115 V RMS 400cps
P18
J18
30 VDC
30VDC(UN-FIL)
55VDC
-12 VDC
+12VDC
22.5VDC
5VPP400CPS
10VPP400CPS
SIG GRD
6
5
7VRMS 400CPS
J20
P 20



4

FIGURE 5 13

TRANSPONDER COMPUTER POWER SCHEMATIC

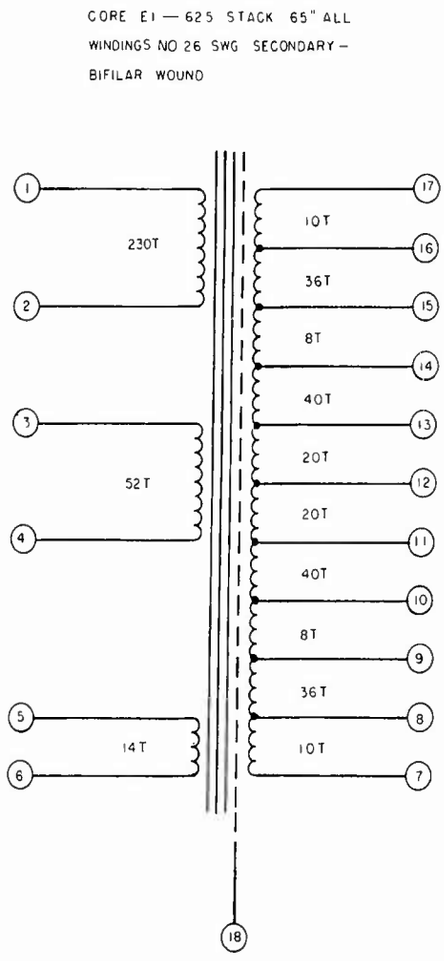
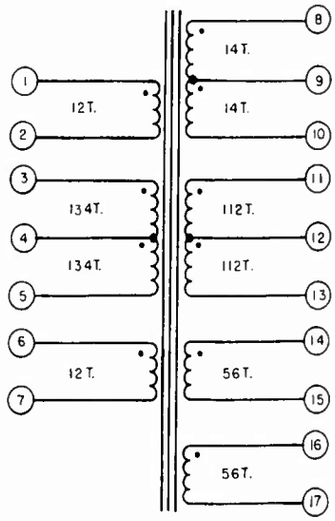


FIGURE 5-14. TRANSPONDER POWER TRANSFORMER



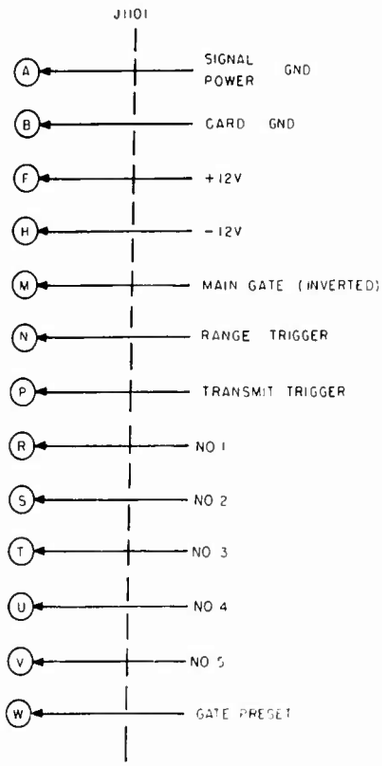
TR -T 100

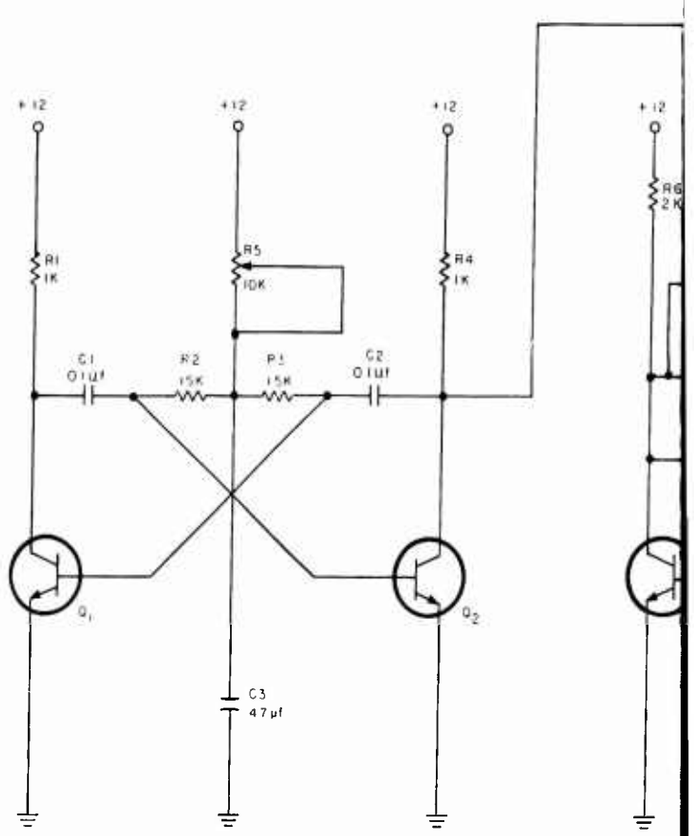
ALL WINDINGS NO.30 SWG

CORE - MAGNETICS INC. ORTHONOL NO.50034, 1 MIL TAPE

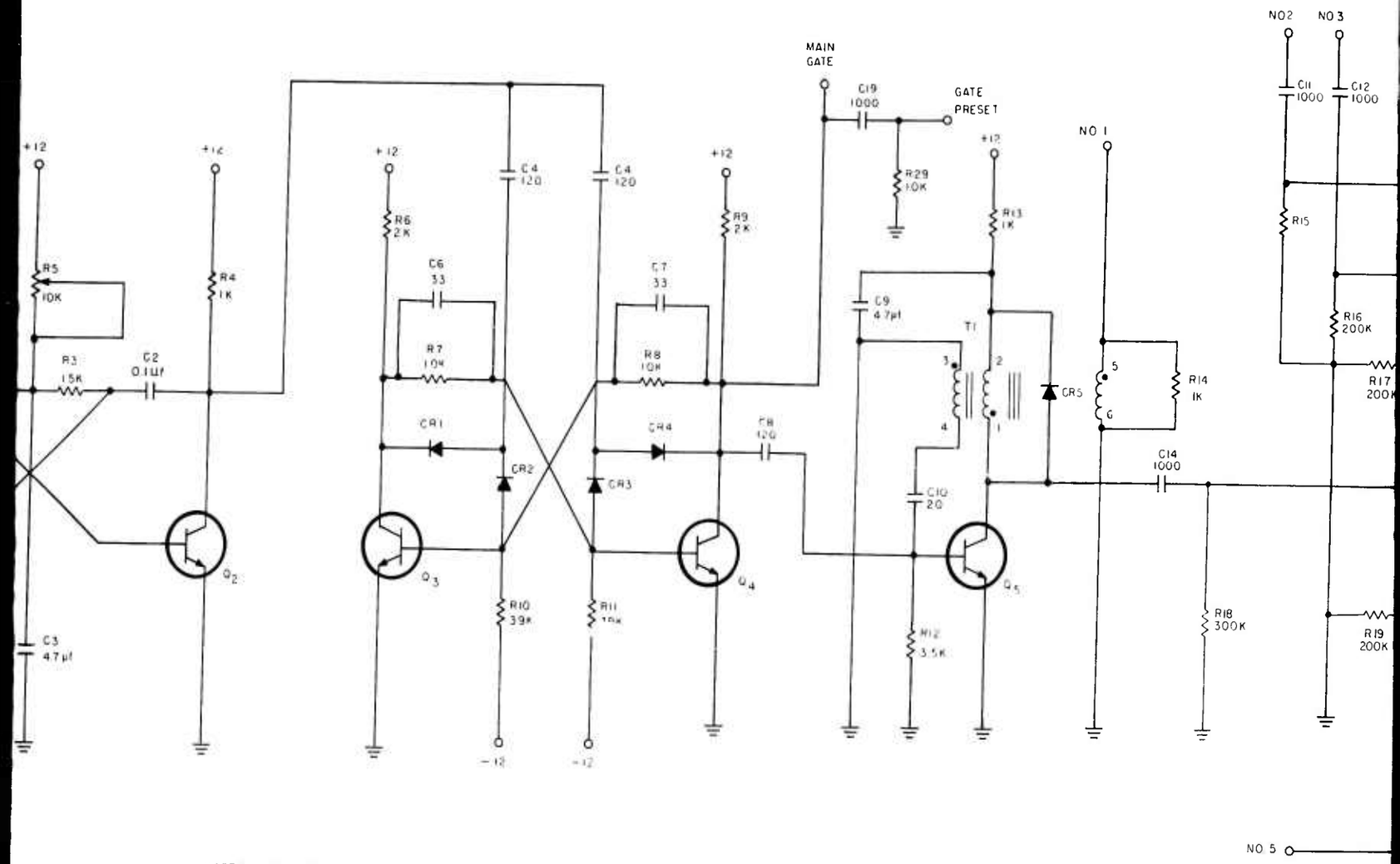
TAPPED WINDINGS ARE BIFILAR WOUND

FIGURE 5-15. INVERTER TRANSFORMER





NOTE 1 ALL RESISTORS IN OH
2 ALL CAPACITORS IN pf
3 ALL DIODES TYPE IN
4 ALL TRANSISTORS TY



NOTE 1 ALL RESISTORS IN OHMS

2 ALL CAPACITORS IN µf UNLESS OTHERWISE SPECIFIED

3 ALL DIODES TYPE IN691

4 ALL TRANSISTORS TYPE 2N708 UNLESS OTHERWISE NOTED

2

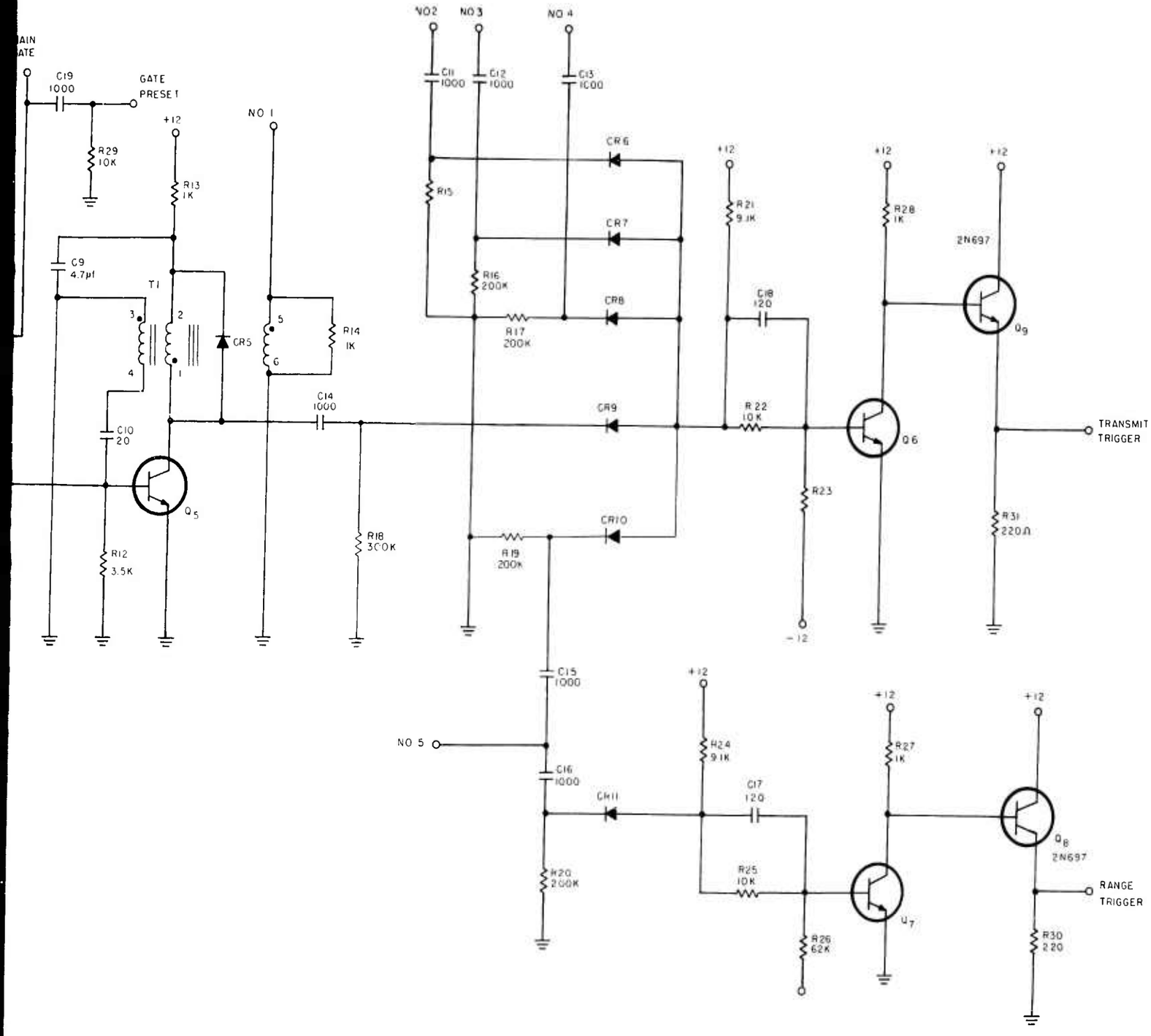
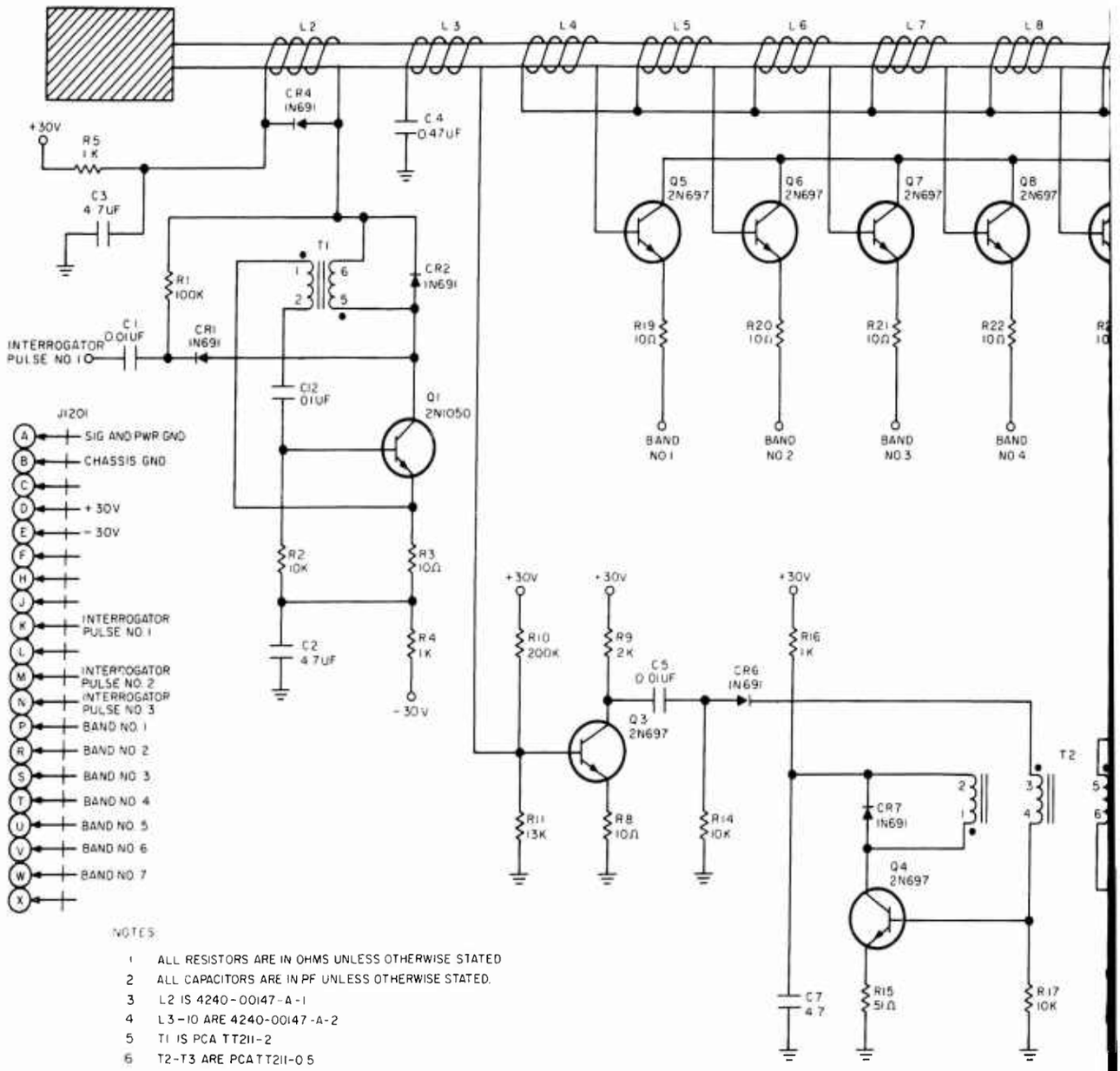


FIGURE 5-16

PULSE AND GATE GENERATOR MIXER AMPLIFIER 1100
CAS SCHEMATIC

3



NOTES

1. ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE STATED
2. ALL CAPACITORS ARE IN PF UNLESS OTHERWISE STATED.
3. L2 IS 4240-00147-A-1
4. L3-10 ARE 4240-00147-A-2
5. T1 IS PCA TT211-2
6. T2-T3 ARE PCA TT211-05

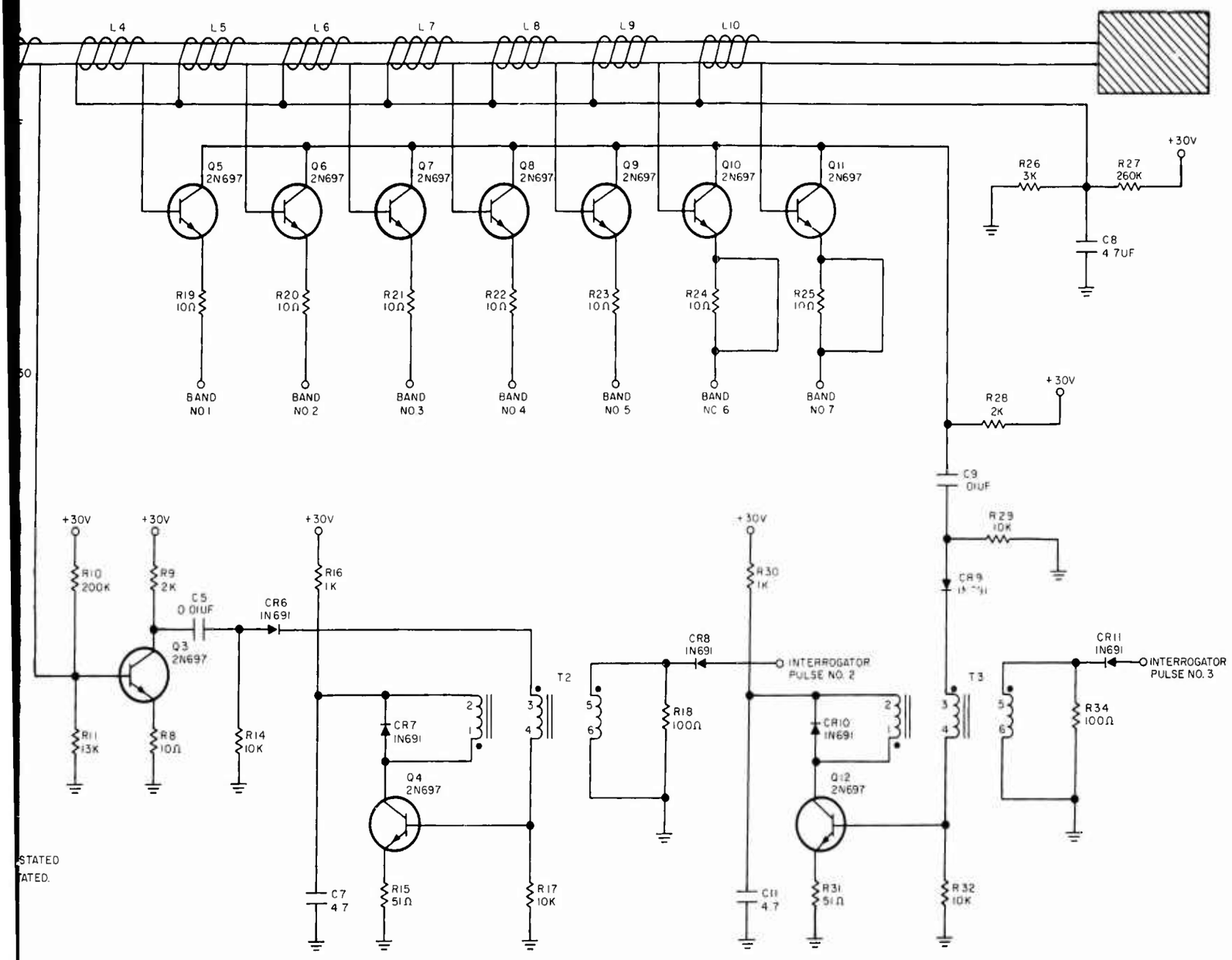
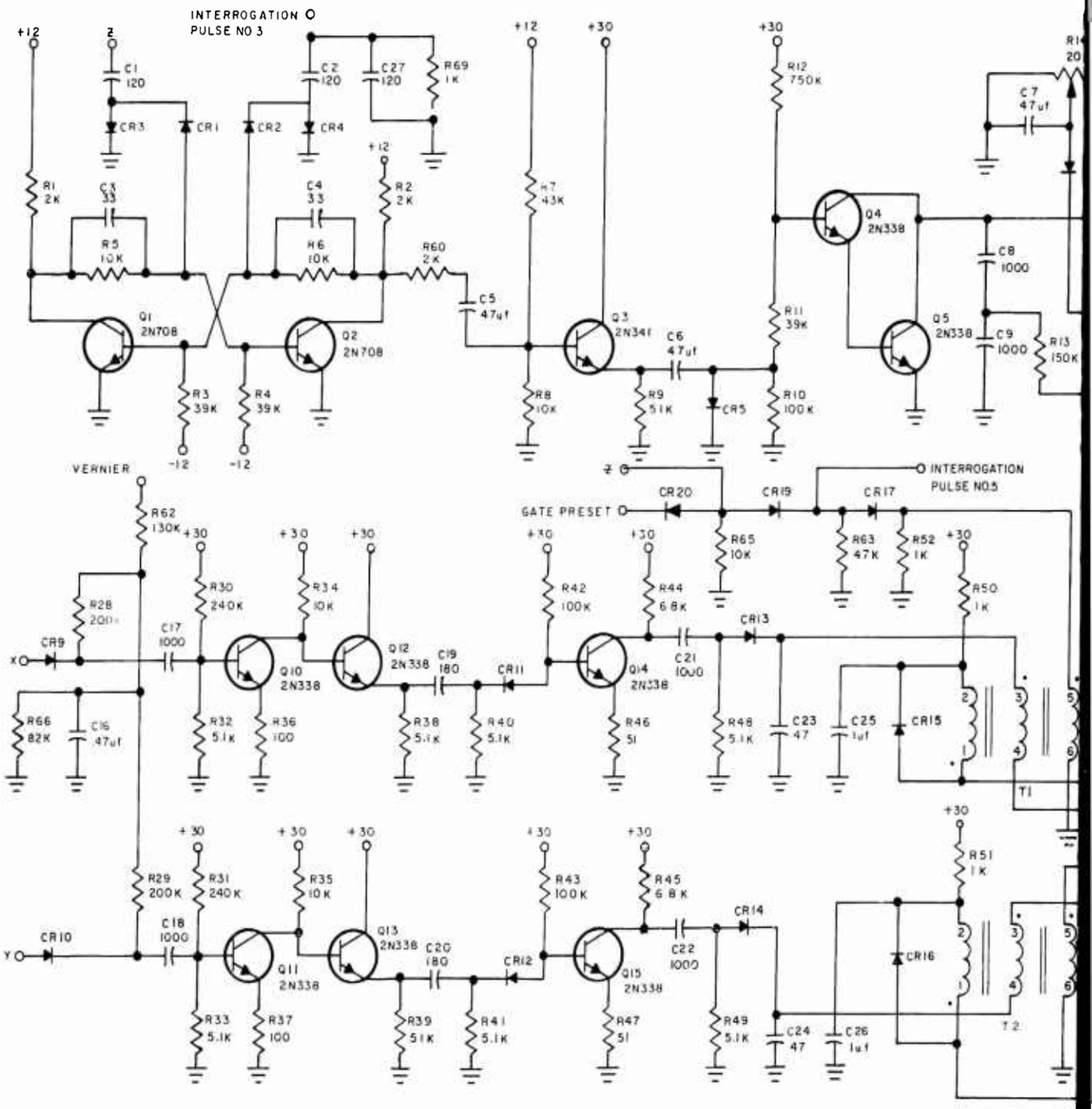
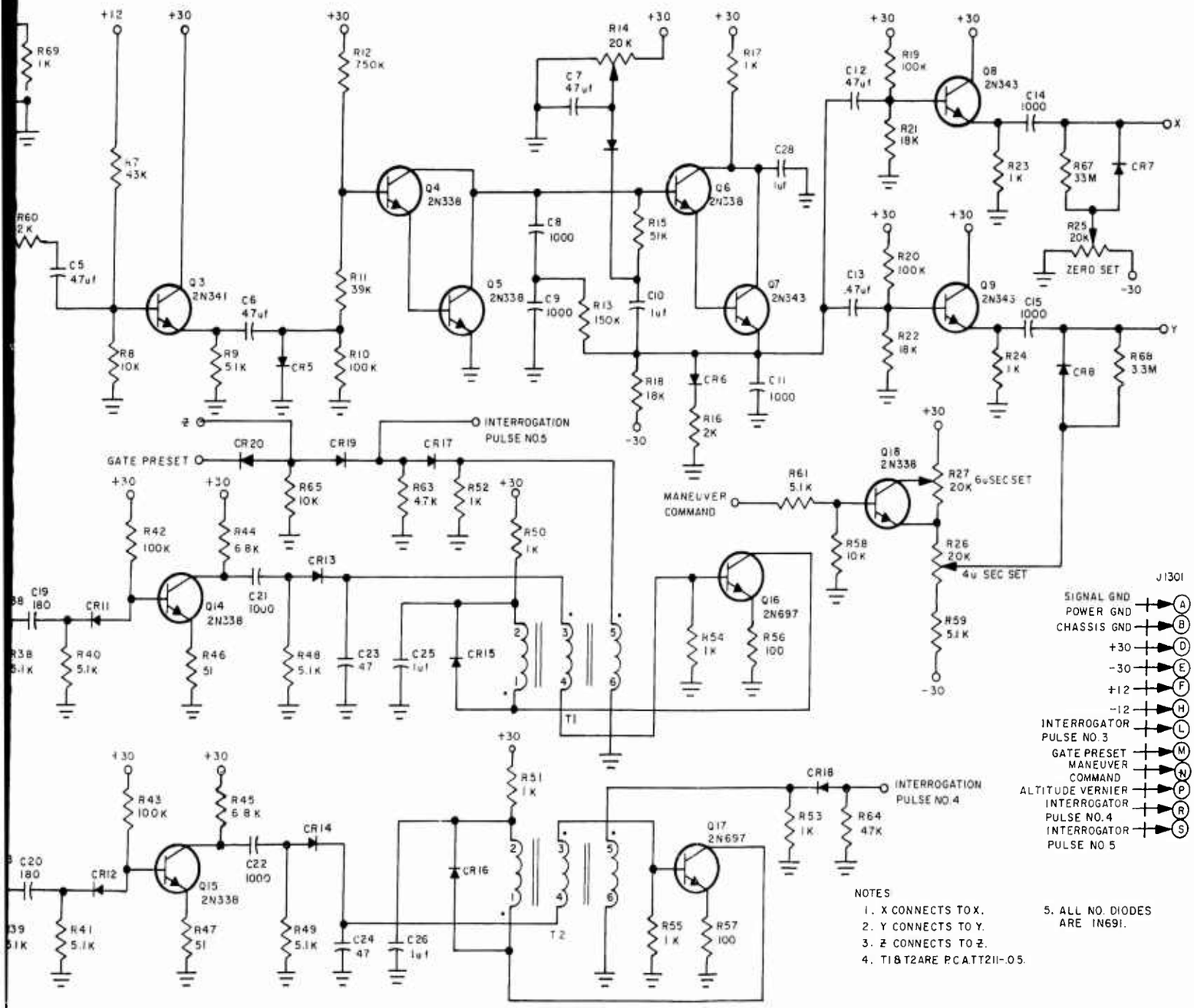


FIGURE 5 17
INTERROGATOR ENCODER CONTROL CODER (1200)


INTERROGATION PULSE NO 3
+12
Z
C1 120
CR3
CR1
CR2
CR4
C2 120
C27 120
R69 1K
R1 2K
C3 33
R5 10K
C4 33
R6 10K
R2 2K
R60 2K
C5 47uf
Q1 2N708
Q2 2N708
R3 39K
R4 39K
-12
+30
R7 43K
R8 10K
Q3 2N341
C6 47uf
R9 51K
CR5
R10 100K
R11 39K
R12 750K
Q4 2N338
Q5 2N338
C7 47uf
C8 1000
C9 1000
R13 150K
R14 20
VERNIER
R62 130K
R28 200K
CR9
X
C17 1000
R30 240K
R34 10K
Q10 2N338
Q12 2N338
C19 180
CR11
R42 100K
R44 6.8K
Q14 2N338
C21 1000
CR13
R66 82K
C16 47uf
R32 5.1K
R36 100
R38 5.1K
R40 5.1K
R46 51
R48 5.1K
C23 47
C25 1uf
CR15
T1
GATE PRESET
CR20
CR19
CR17
R65 10K
R63 47K
R52 1K
R50 1K
INTERROGATION PULSE NO.5
R29 200K
CR10
Y
C18 1000
R31 240K
R35 10K
Q11 2N338
Q13 2N338
C20 180
CR12
R43 100K
R45 6.8K
Q15 2N338
C22 1000
CR14
R51 1K
CR16
T2
R33 5.1K
R37 100
R39 5.1K
R41 5.1K
R47 51
R49 5.1K
C24 47
C26 1uf

1

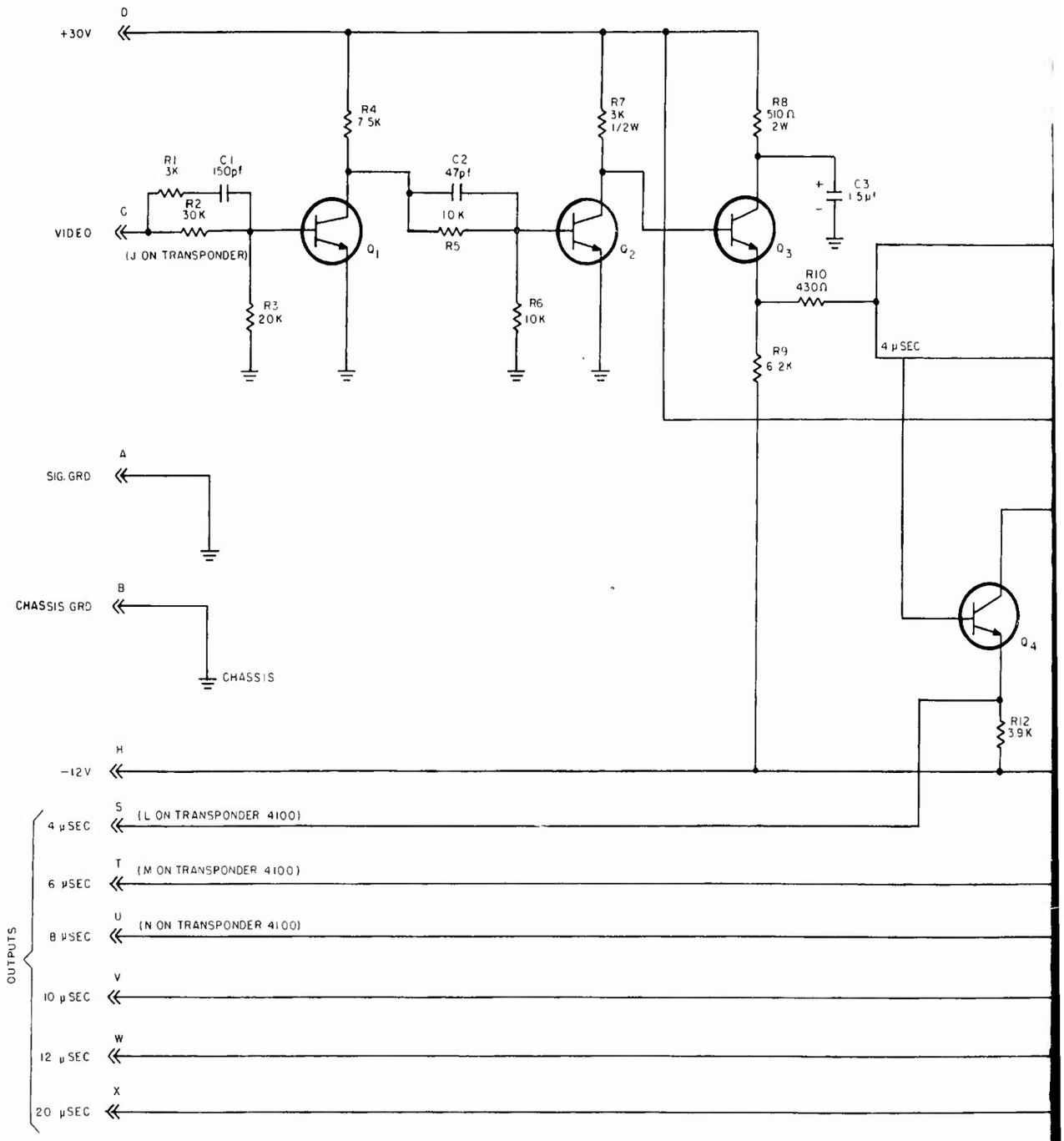


NOTES

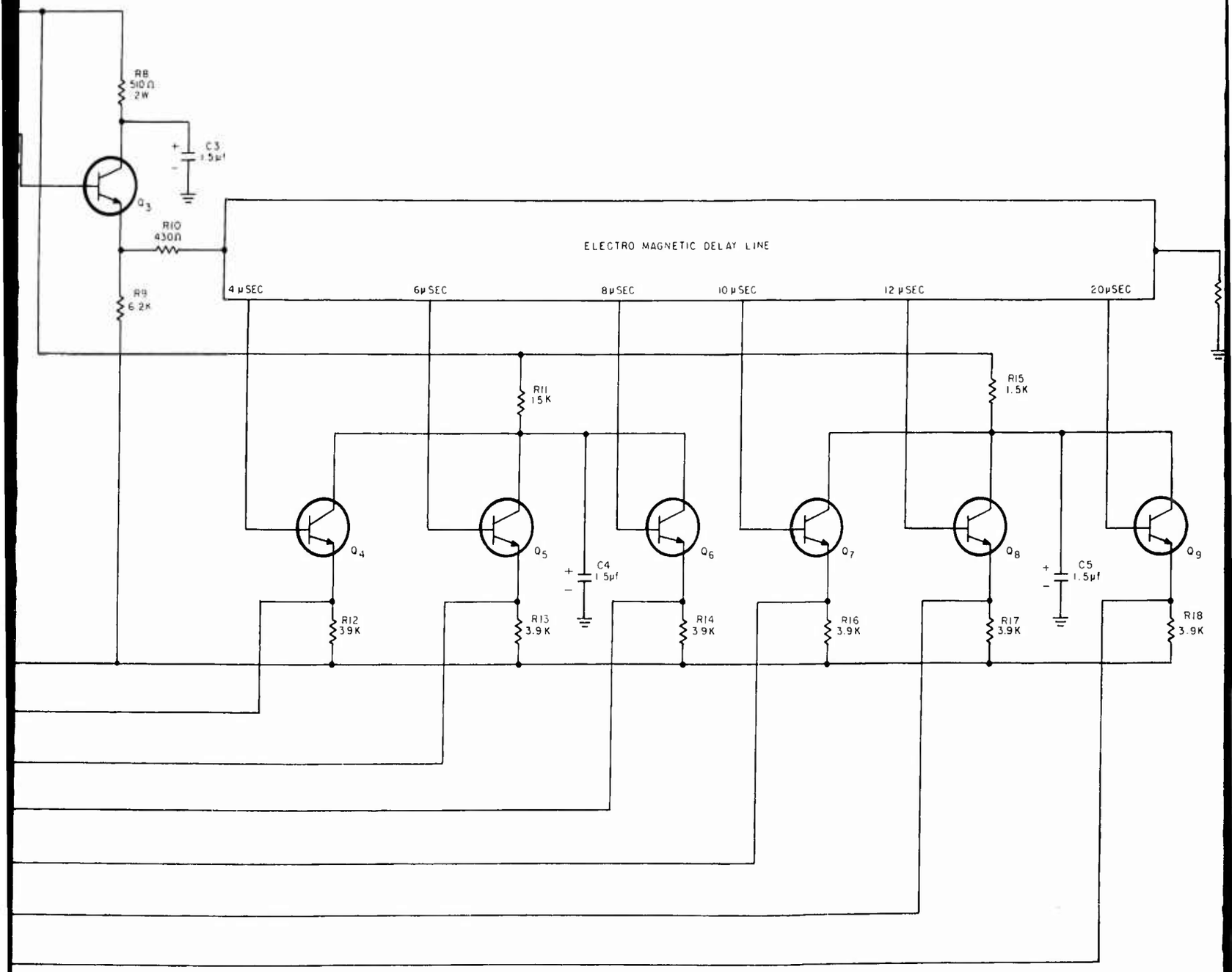
1. X CONNECTS TO X.
2. Y CONNECTS TO Y.
3. Z CONNECTS TO Z.
4. T1 & T2 ARE P.C. ATT211-05.
5. ALL NO. DIODES ARE IN691.

FIGURE 5-18

VERNIER CODER (1300)



NOTE Q_7, Q_8, & Q_9, AND OUTPUTS (10 μSEC, 12 μSEC, 20 μSEC) DO NOT EXIST ON TRANSPONDER DECODER DELAY L



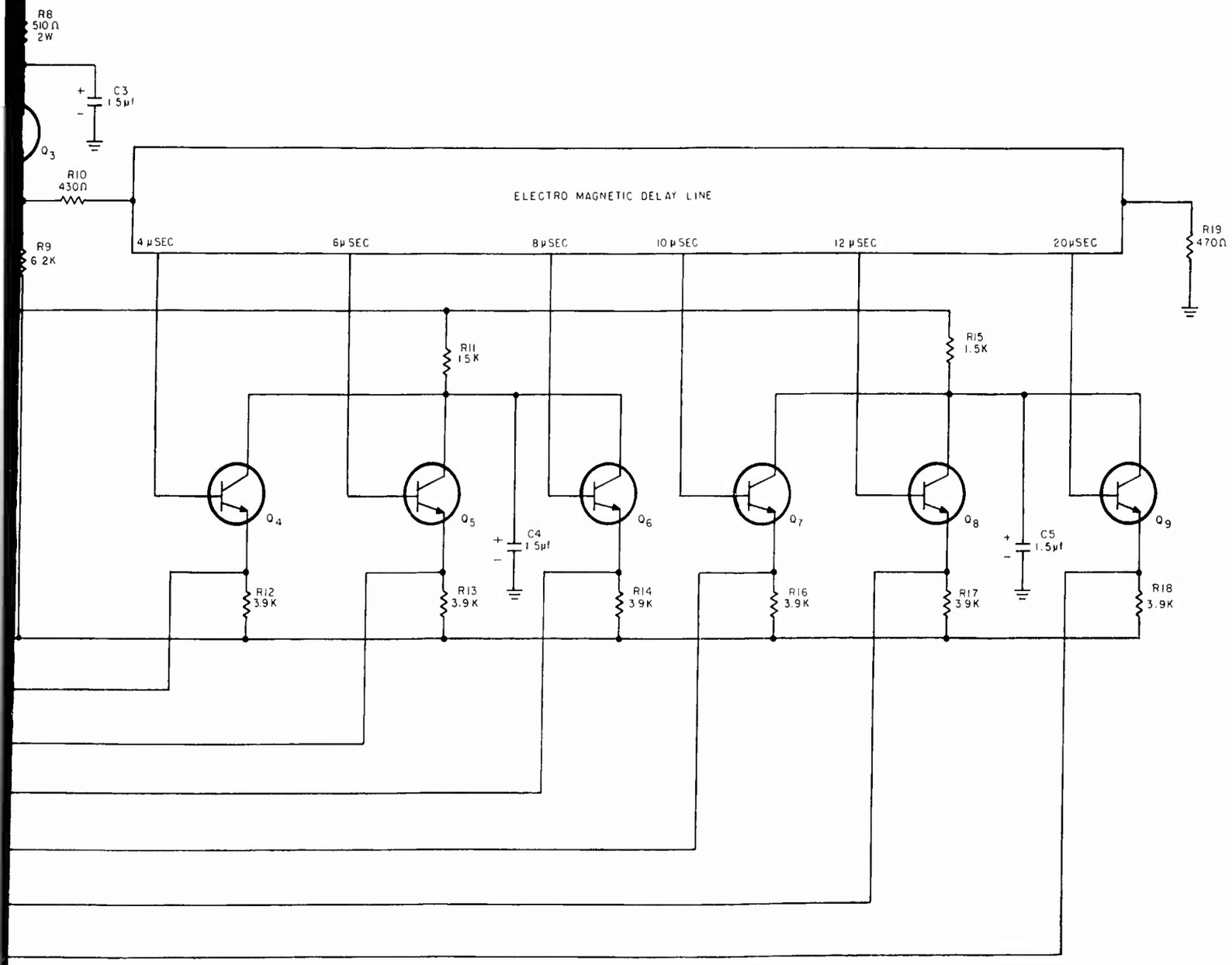
, 20 μSEC) DO NOT EXIST ON TRANSPONDER DECODER DELAY LINE CHASSIS 4100.

Q_1 Q_4 — — — Q_9 — — — — 2N1104 OR 2N338
Q_2 — — — — — — — — 2N708
Q_3 — — — — — — — — 2N699

FIGURE 5-19

DECODER DELAY LINE AND DRIVER (INTERROGATO
TRANSPONDER) (2100 AND 4100)

2



NOT EXIST ON TRANSPONDER DECODER DELAY LINE CHASSIS 4100.

Q_1 Q_4 — — — Q_9 — — — — 2N1104 OR 2N338

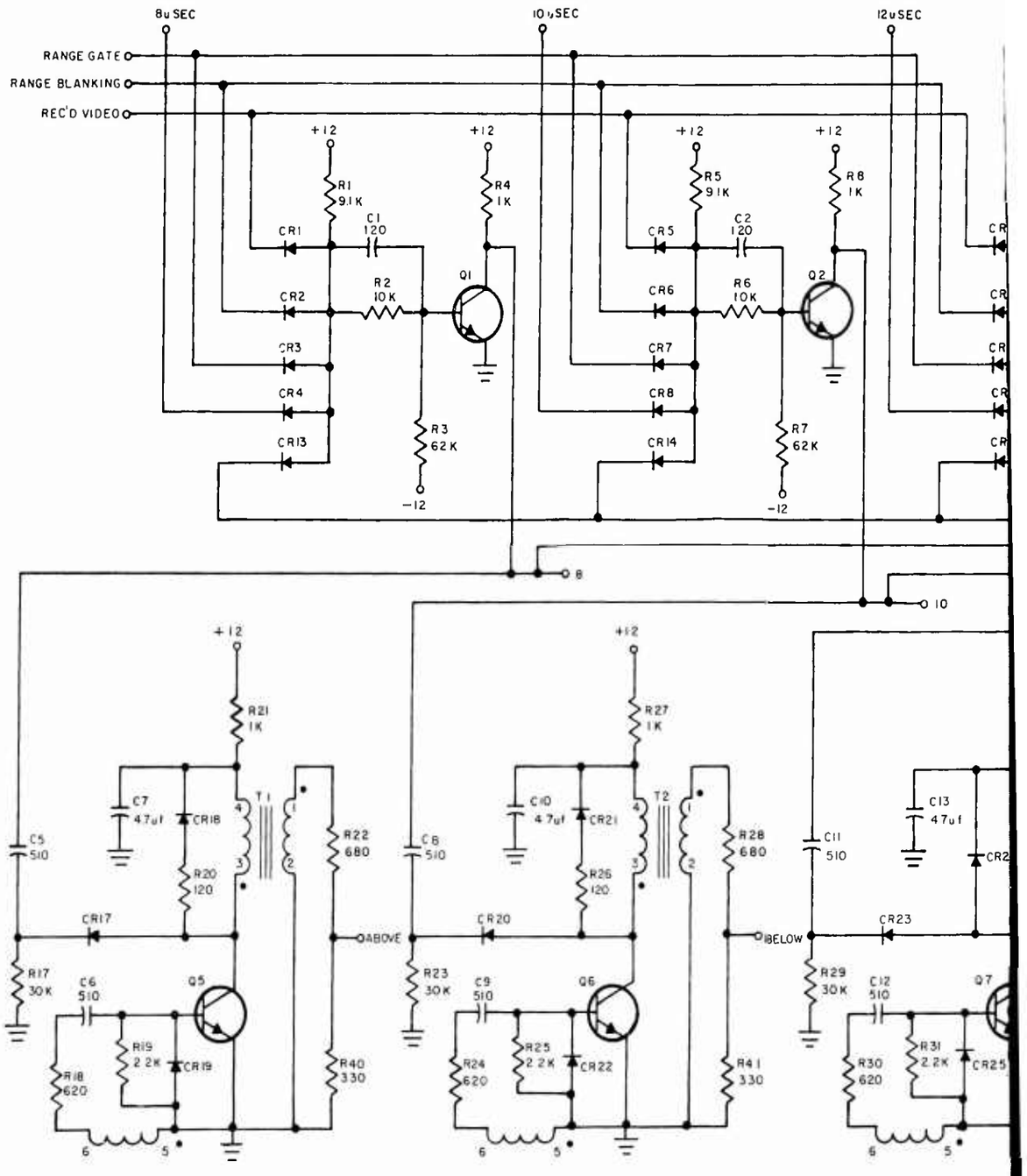
Q_2 — — — — — — — — — 2N708

Q_3 — — — — — — — — — 2N699

3

FIGURE 5-19

DECODER DELAY LINE AND DRIVER (INTERROGATOR-TRANSPONDER) (2100 AND 4100)


8uSEC
10uSEC
12uSEC
RANGE GATE
RANGE BLANKING
REC'D VIDEO
+12
R1 9.1K
R4 1K
C1 120
CR1
CR2
R2 10K
Q1
CR3
CR4
CR13
R3 62K
-12
R5 9.1K
R8 1K
C2 120
CR5
CR6
R6 10K
Q2
CR7
CR8
CR14
R7 62K
8
10
R21 1K
C7 4.7uf
CR18
T1
R22 680
C5 510
R20 120
CR17
ABOVE
R17 30K
C6 510
Q5
R19 2.2K
CR19
R18 620
R40 330
R27 1K
C10 4.7uf
CR21
T2
R28 680
C8 510
R26 120
CR20
R23 30K
C9 510
Q6
R25 2.2K
CR22
R24 620
R41 330
C11 510
C13 4.7uf
CR23
BELOW
R29 30K
C12 510
Q7
R31 2.2K
CR25
R30 620

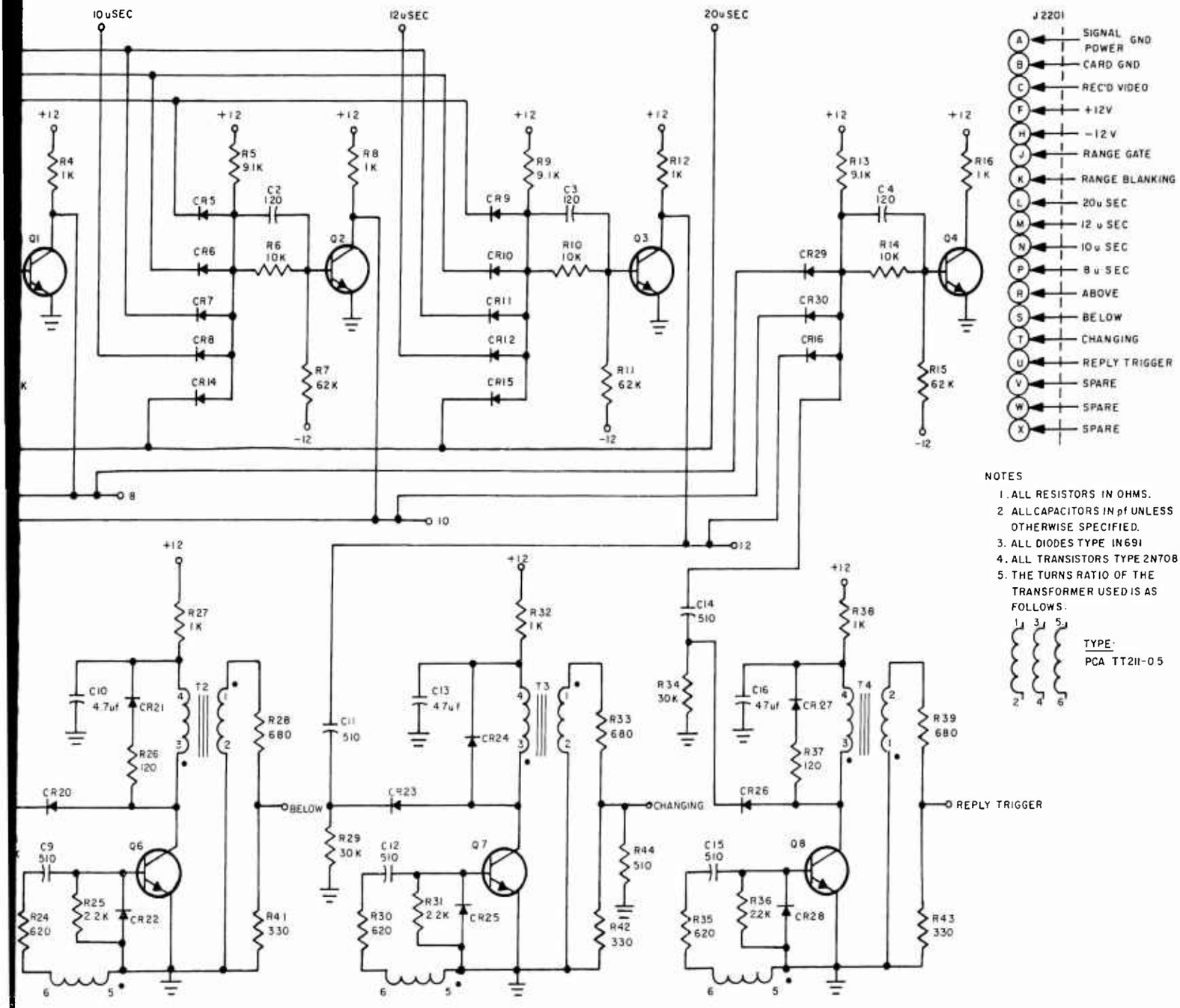
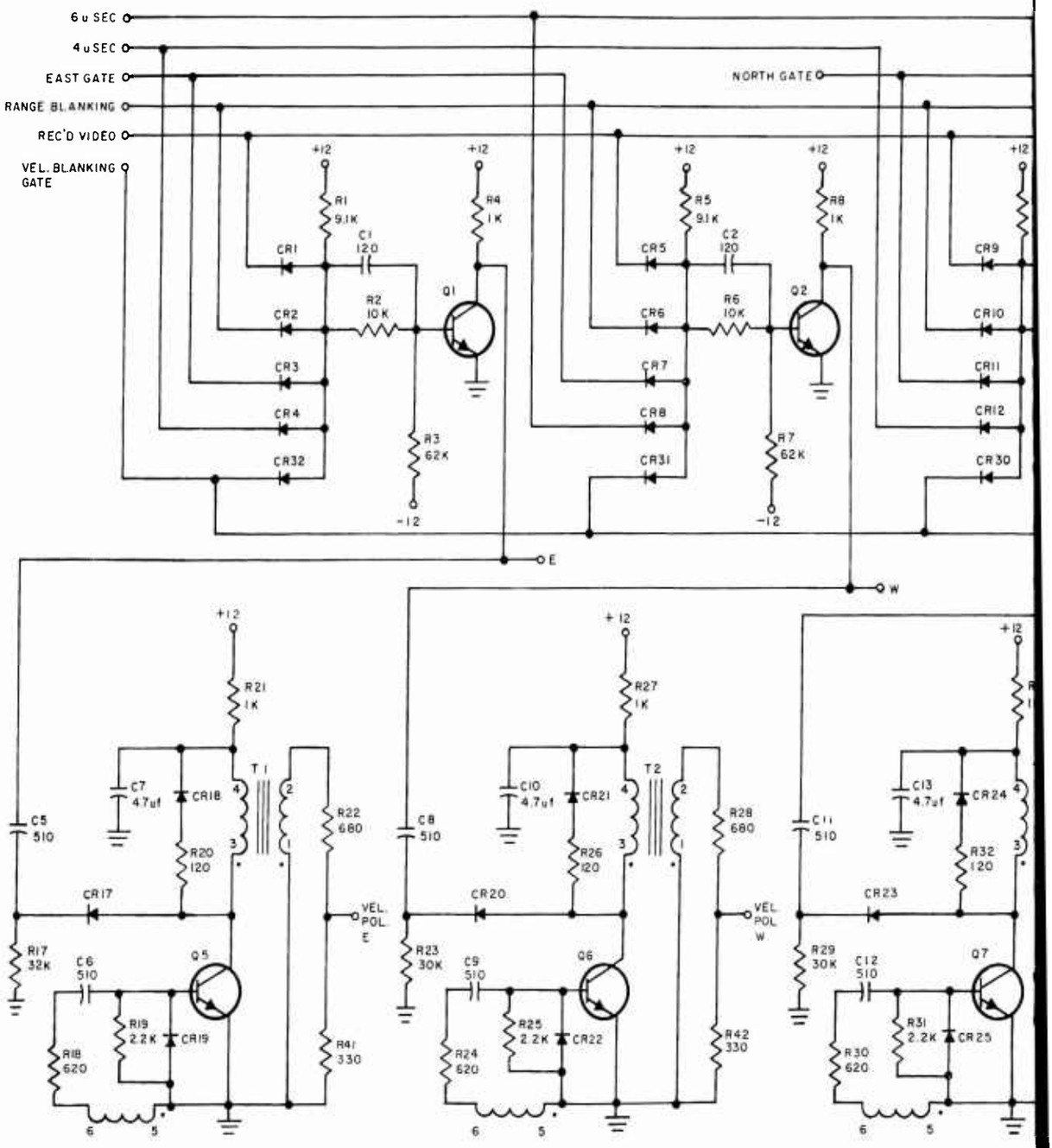


FIGURE 5-20.

RELATIVE ALTITUDE VELOCITY SCALE DECODER (2200)


6 u SEC
4 u SEC
EAST GATE
RANGE BLANKING
REC'D VIDEO
VEL. BLANKING GATE
NORTH GATE
+12
R1 9.1K
C1 120
CR1
CR2
CR3
CR4
CR32
R2 10K
Q1
R3 62K
-12
R4 1K
R5 9.1K
C2 120
CR5
CR6
CR7
CR8
CR31
R6 10K
Q2
R7 62K
R8 1K
CR9
CR10
CR11
CR12
CR30
E
W
R21 1K
C7 4.7uf
CR18
T1
R20 120
C5 510
CR17
R17 32K
C6 510
Q5
R19 2.2K
CR19
R18 620
R22 680
R41 330
VEL. POL. E
R27 1K
C10 4.7uf
CR21
T2
R26 120
C8 510
CR20
R23 30K
C9 510
Q6
R25 2.2K
CR22
R24 620
R28 680
R42 330
VEL. POL. W
C13 4.7uf
CR24
R32 120
C11 510
CR23
R29 30K
C12 510
Q7
R31 2.2K
CR25
R30 620


1

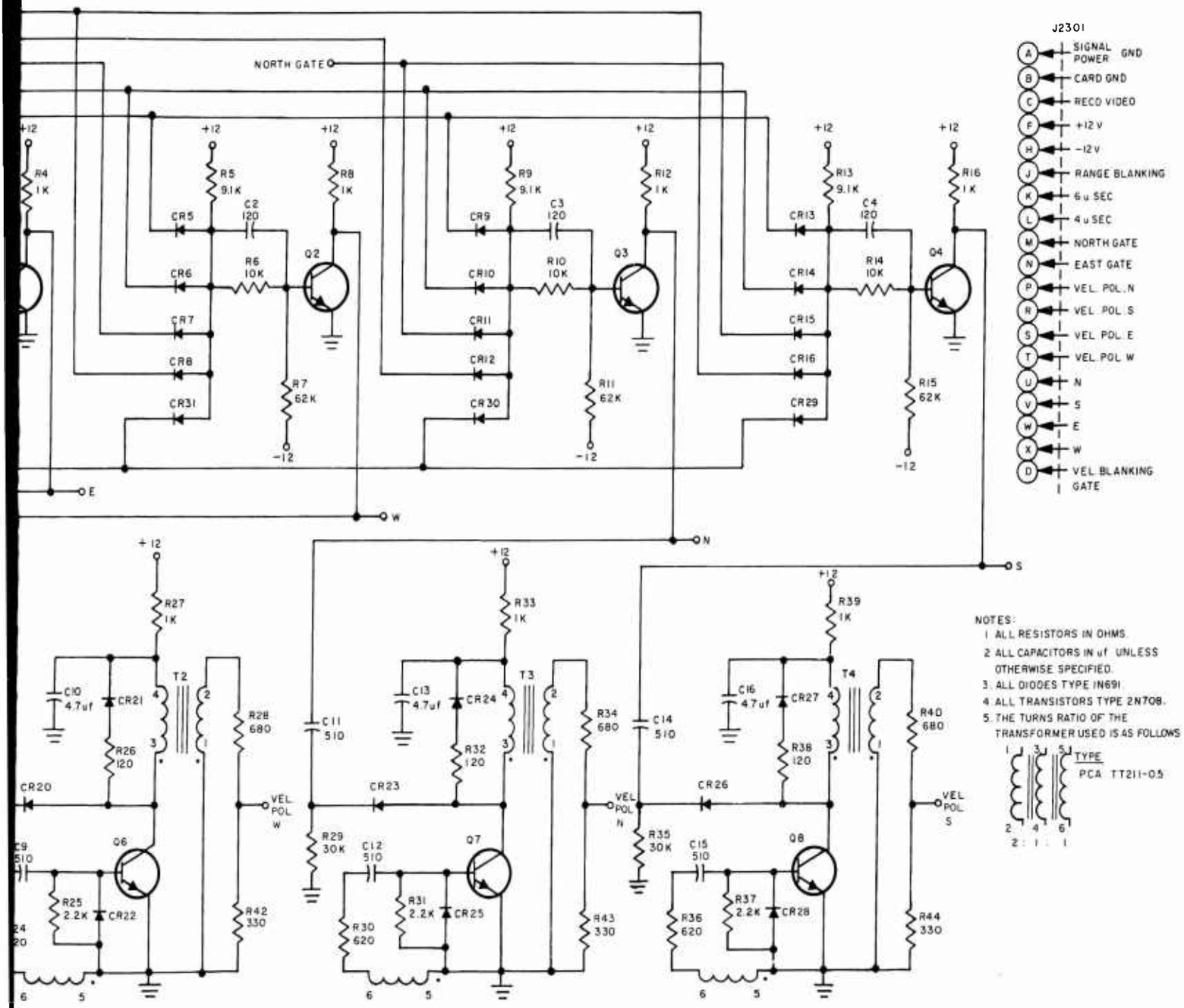
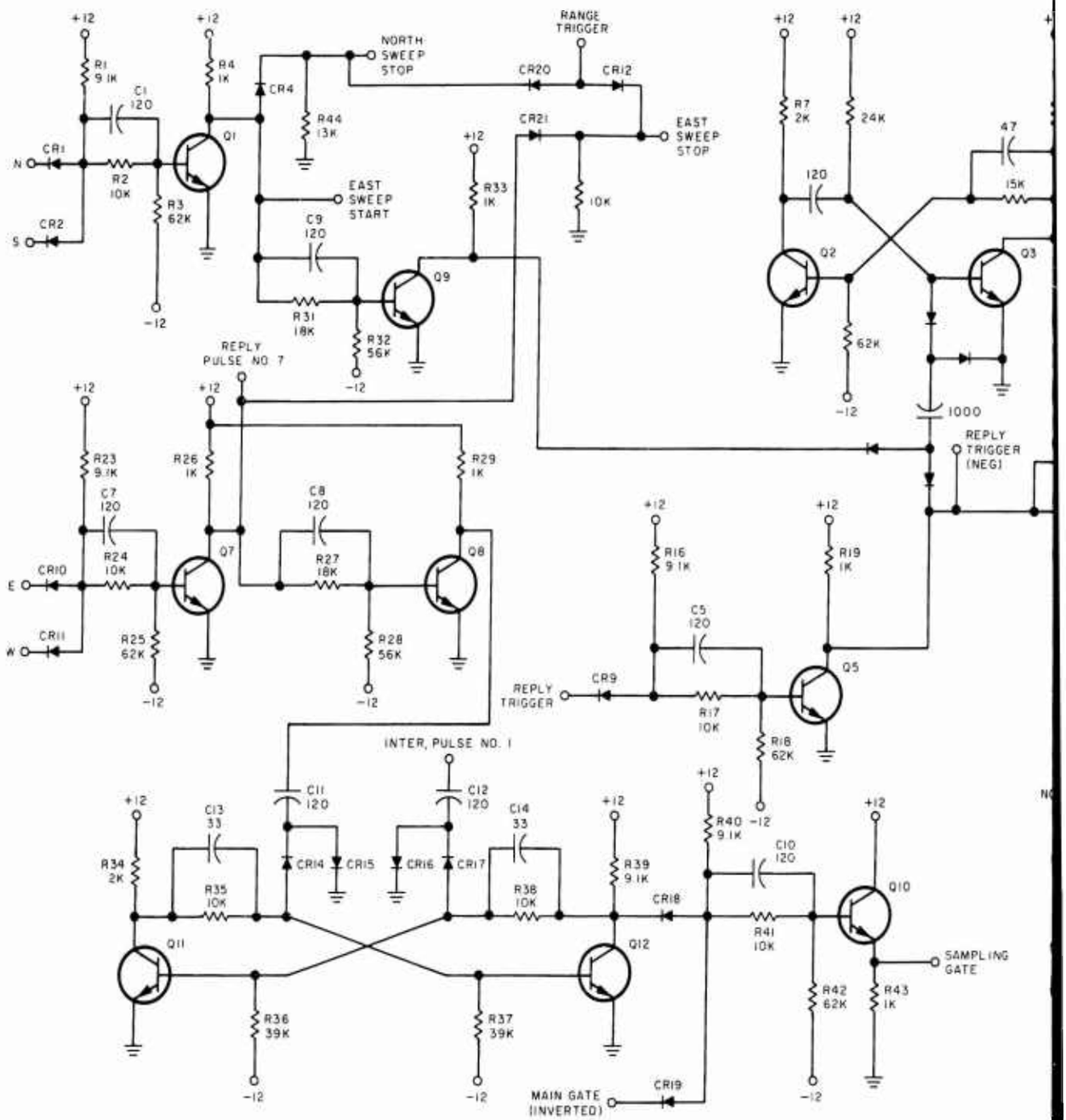
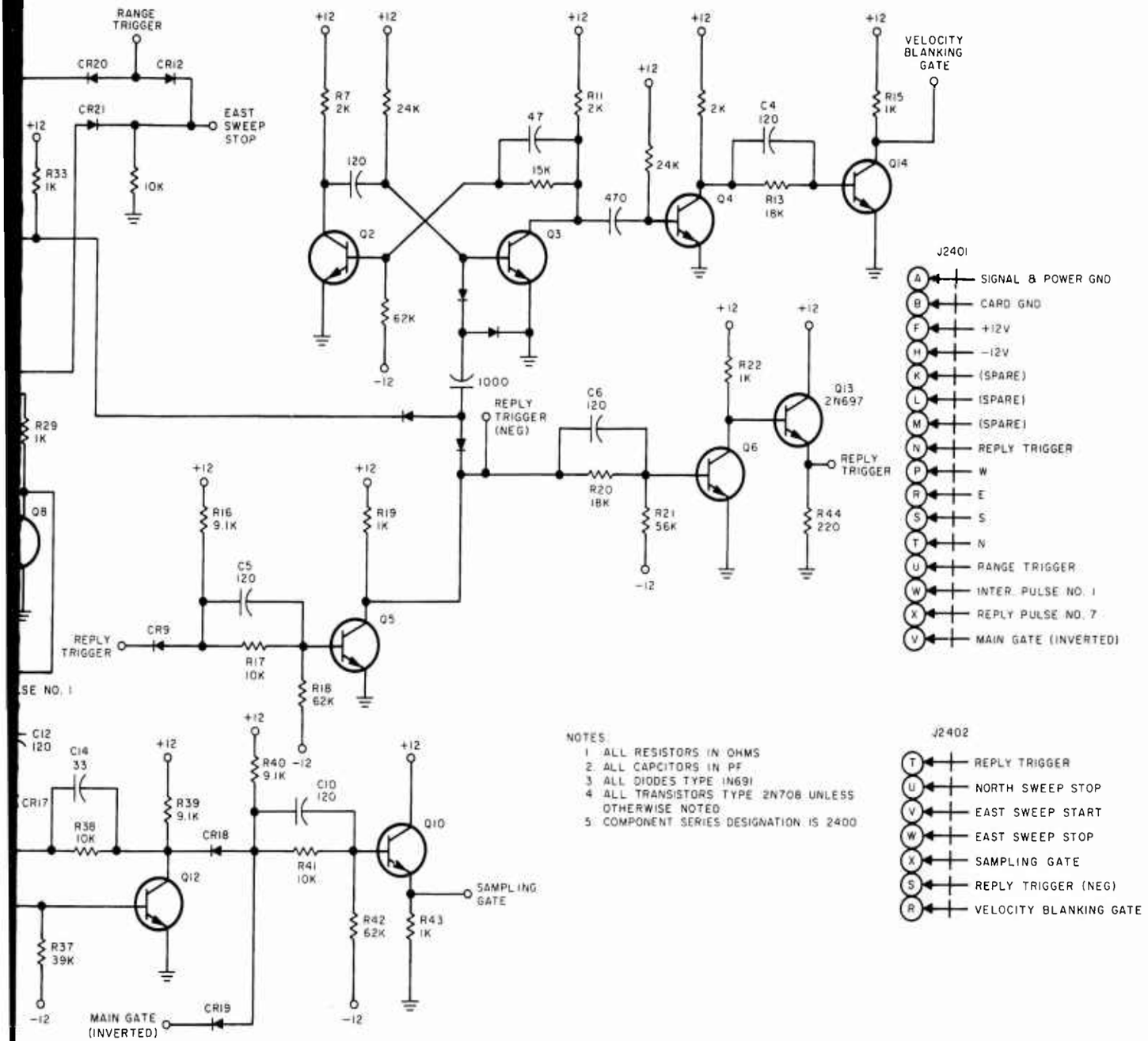


FIGURE 5-21

VELOCITY POLARITY DECODER (2300)


+12
R1 9.1K
C1 120
CR1
N
R2 10K
R3 62K
-12
CR2
S
R4 1K
Q1
CR4
R44 13K
NORTH SWEEP STOP
RANGE TRIGGER
CR20
CR12
CR21
EAST SWEEP STOP
EAST SWEEP START
R33 1K
10K
C9 120
Q9
R31 18K
R32 56K
REPLY PULSE NO. 7
R7 2K
24K
47
120
15K
Q2
Q3
62K
1000
REPLY TRIGGER (NEG)
R23 9.1K
C7 120
R24 10K
CR10
E
CR11
W
R25 62K
R26 1K
Q7
C8 120
R27 18K
R28 56K
R29 1K
Q8
R16 9.1K
R19 1K
C5 120
Q5
REPLY TRIGGER
CR9
R17 10K
R18 62K
INTER. PULSE NO. 1
C11 120
C12 120
C13 33
C14 33
R34 2K
R35 10K
CR14
CR15
CR16
CR17
R38 10K
R39 9.1K
R40 9.1K
C10 120
CR18
R41 10K
Q10
Q11
Q12
SAMPLING GATE
R36 39K
R37 39K
R42 62K
R43 1K
MAIN GATE (INVERTED)
CR19

1

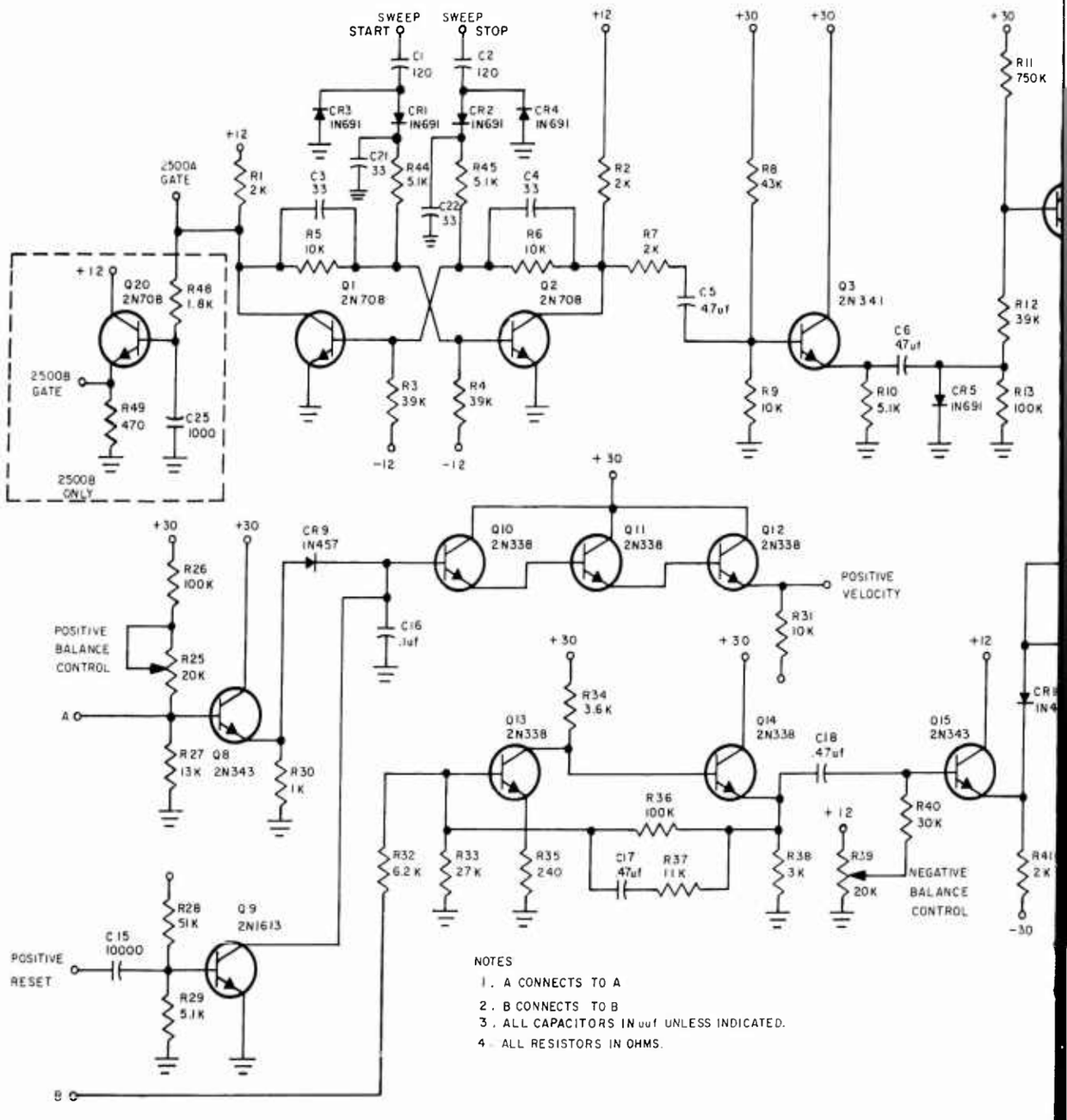


NOTES
1. ALL RESISTORS IN OHMS
2. ALL CAPCITORS IN PF
3. ALL DIODES TYPE IN691
4. ALL TRANSISTORS TYPE 2N708 UNLESS OTHERWISE NOTED
5. COMPONENT SERIES DESIGNATION IS 2400

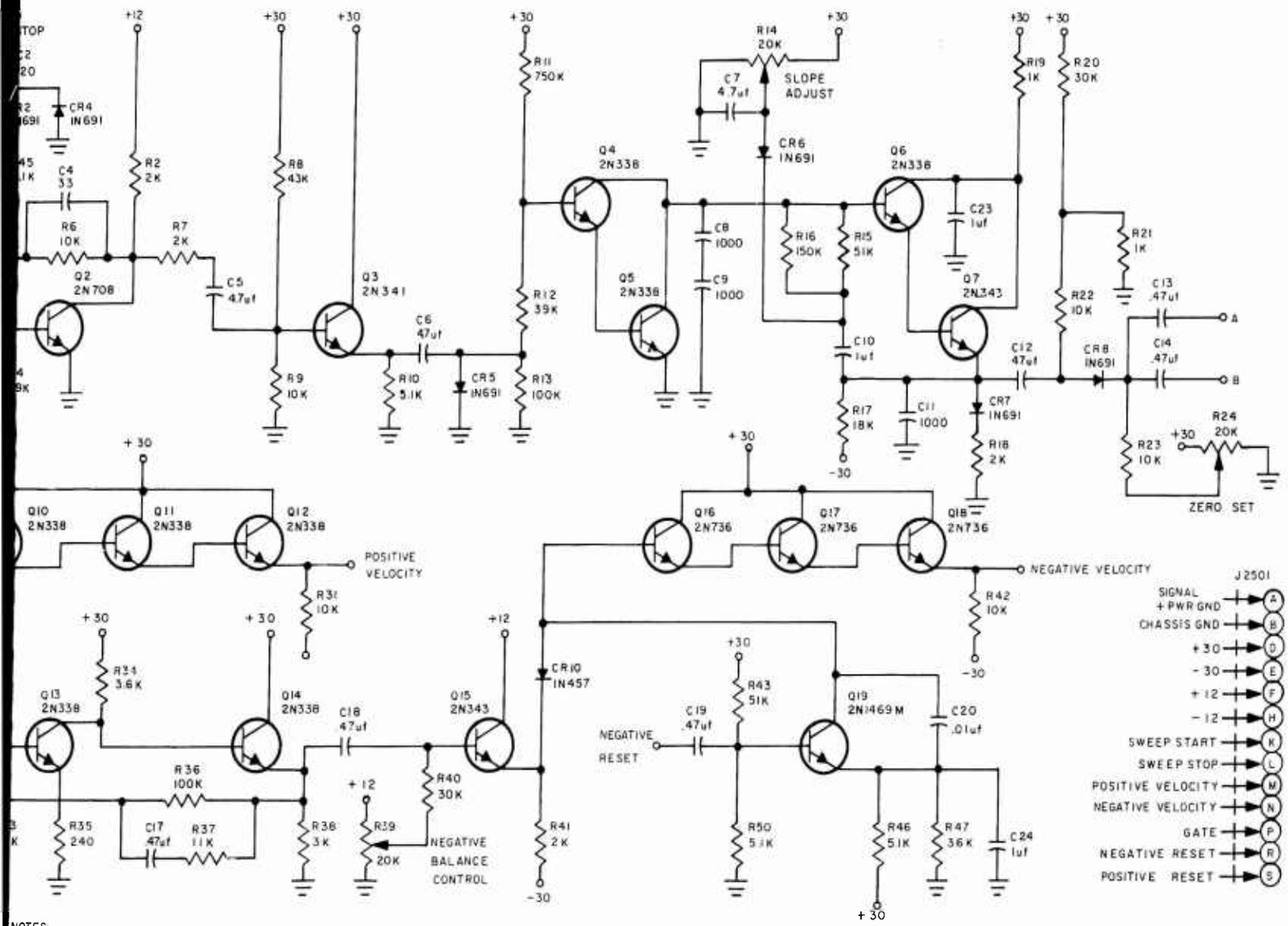
2

FIGURE 5 22

PULSE SELECTOR (2400)


SWEEP START
SWEEP STOP
C1 120
C2 120
CR3 IN691
CR1 IN691
CR2 IN691
CR4 IN691
+12
+30
+30
+30
R11 750K
2500A GATE
R1 2K
C3 33
C21 33
R44 5.1K
R45 5.1K
C4 33
C22 33
R2 2K
R8 43K
R5 10K
R6 10K
R7 2K
Q1 2N708
Q2 2N708
C5 47uf
Q3 2N341
C6 47uf
R12 39K
+12
Q20 2N708
R48 1.8K
2500B GATE
R49 470
C25 1000
2500B ONLY
R3 39K
R4 39K
-12
-12
R9 10K
R10 5.1K
CR5 IN691
R13 100K
+30
+30
+30
CR9 IN457
Q10 2N338
Q11 2N338
Q12 2N338
POSITIVE VELOCITY
R26 100K
POSITIVE BALANCE CONTROL
R25 20K
C16 .1uf
R31 10K
+30
+30
+12
A
R34 3.6K
Q13 2N338
Q14 2N338
C18 .47uf
Q15 2N343
R27 13K
Q8 2N343
R30 1K
R36 100K
R40 30K
+12
R32 6.2K
R33 27K
R35 240
C17 47uf
R37 11K
R38 3K
R39 20K
NEGATIVE BALANCE CONTROL
-30
R28 51K
Q9 2N1613
C15 10000
POSITIVE RESET
R29 5.1K
B
NOTES
1. A CONNECTS TO A
2. B CONNECTS TO B
3. ALL CAPACITORS IN uuf UNLESS INDICATED.
4. ALL RESISTORS IN OHMS.

1



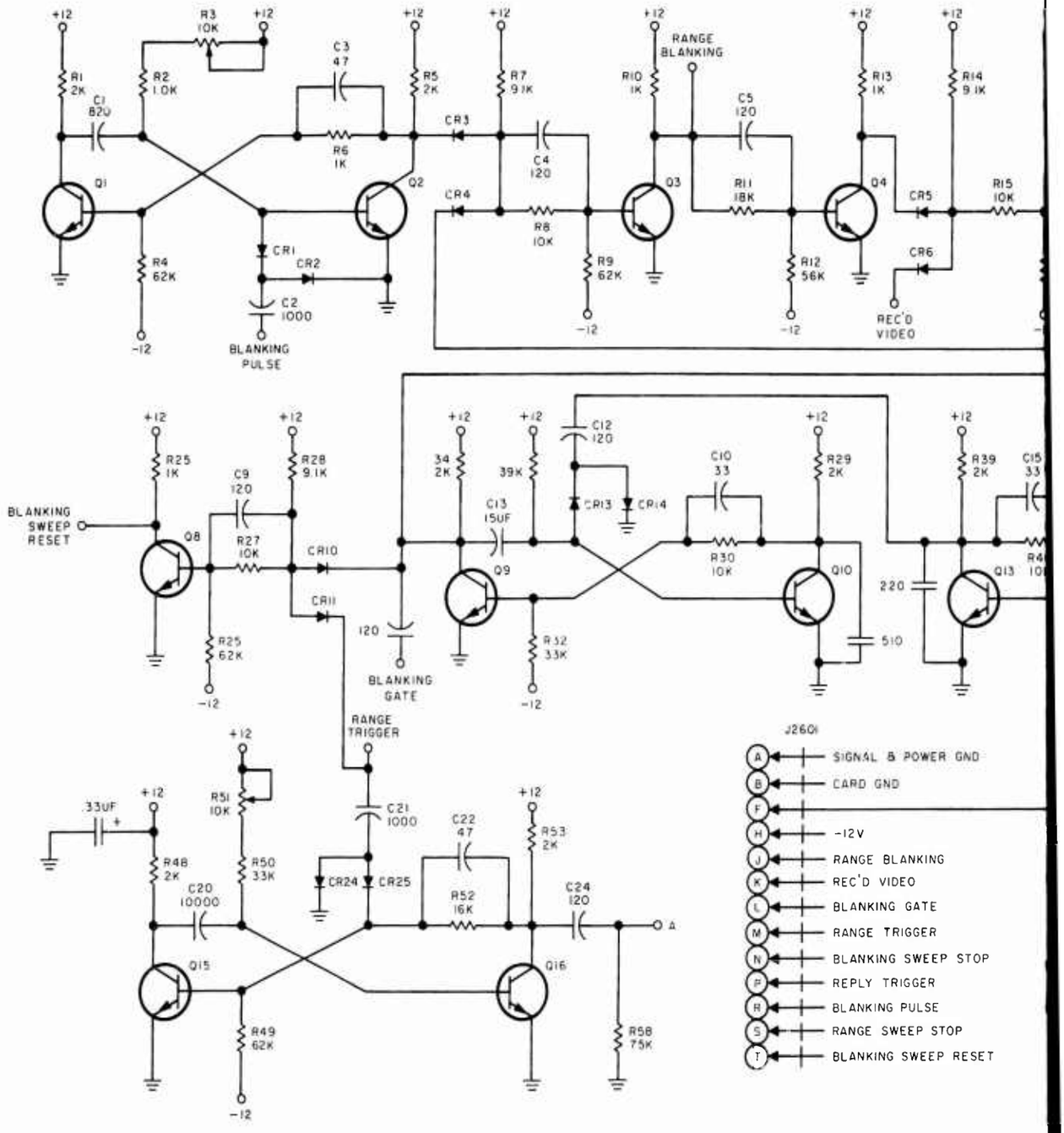
NOTES:

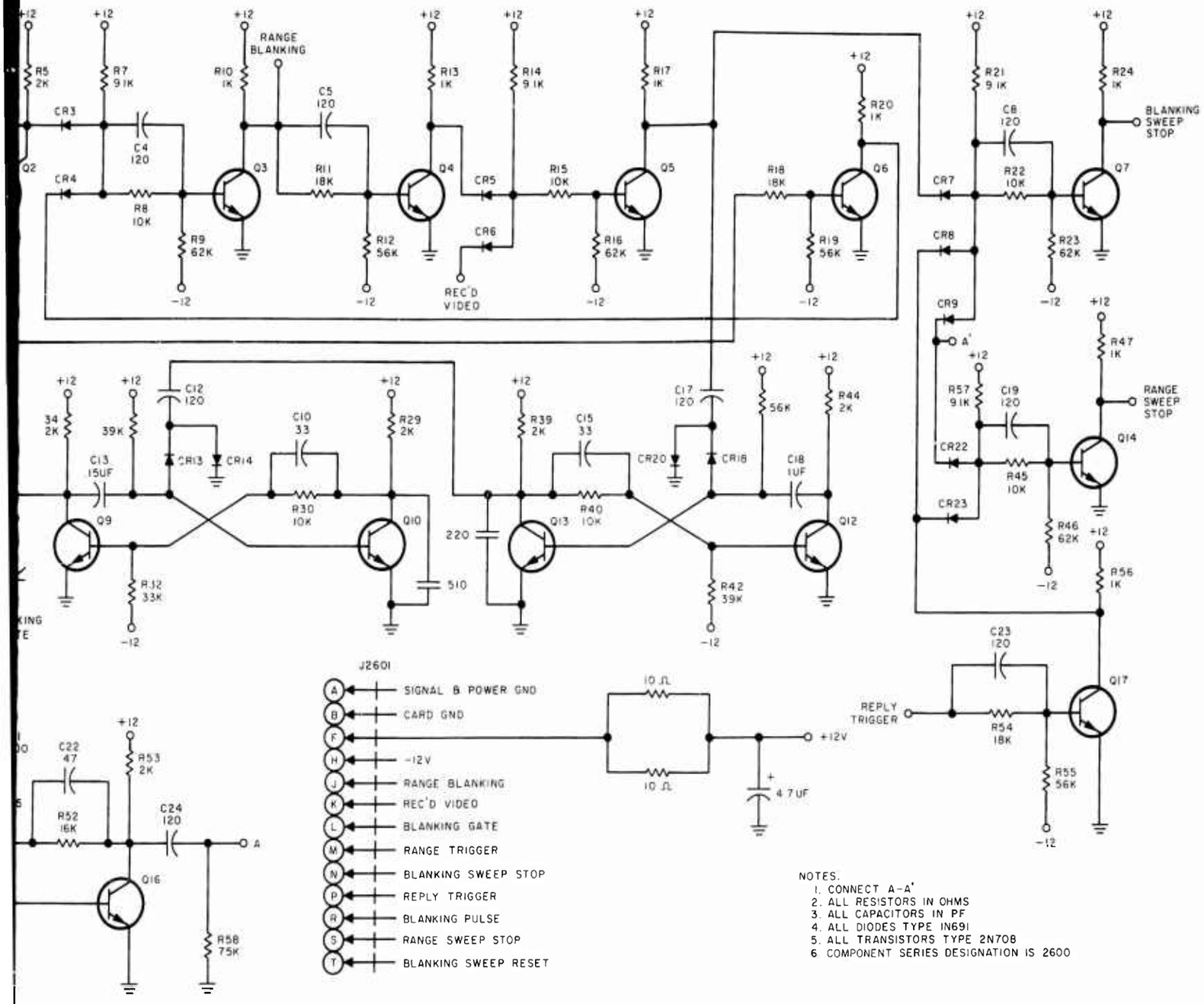
1. A CONNECTS TO A
2. B CONNECTS TO B
3. ALL CAPACITORS IN uuf UNLESS INDICATED.
4. ALL RESISTORS IN OHMS.

2

FIGURE 5-23

NORTH EAST VELOCITY DECODER (2500)


+12
R1 2K
C1 820
R2 1.0K
R3 10K
C3 47
R6 1K
R5 2K
R7 9.1K
CR3
C4 120
CR4
R8 10K
R9 62K
-12
Q1
Q2
R4 62K
CR1
CR2
C2 1000
BLANKING PULSE
RANGE BLANKING
R10 1K
C5 120
R11 18K
R12 56K
Q3
Q4
R13 1K
R14 9.1K
CR5
CR6
R15 10K
REC'D VIDEO
BLANKING SWEEP RESET
R25 1K
C9 120
R28 9.1K
Q8
R27 10K
CR10
CR11
R25 62K
120
BLANKING GATE
34 2K
39K
C12 120
C13 15UF
CR13
CR14
Q9
R32 33K
C10 33
R30 10K
R29 2K
Q10
510
R39 2K
C15 33
220
Q13
RANGE TRIGGER
.33UF
R51 10K
R48 2K
R50 33K
C20 10000
C21 1000
CR24
CR25
C22 47
R52 16K
R53 2K
C24 120
A
Q15
Q16
R49 62K
R58 75K
J2601
A SIGNAL & POWER GND
B CARD GND
F
H -12V
J RANGE BLANKING
K REC'D VIDEO
L BLANKING GATE
M RANGE TRIGGER
N BLANKING SWEEP STOP
P REPLY TRIGGER
R BLANKING PULSE
S RANGE SWEEP STOP
T BLANKING SWEEP RESET

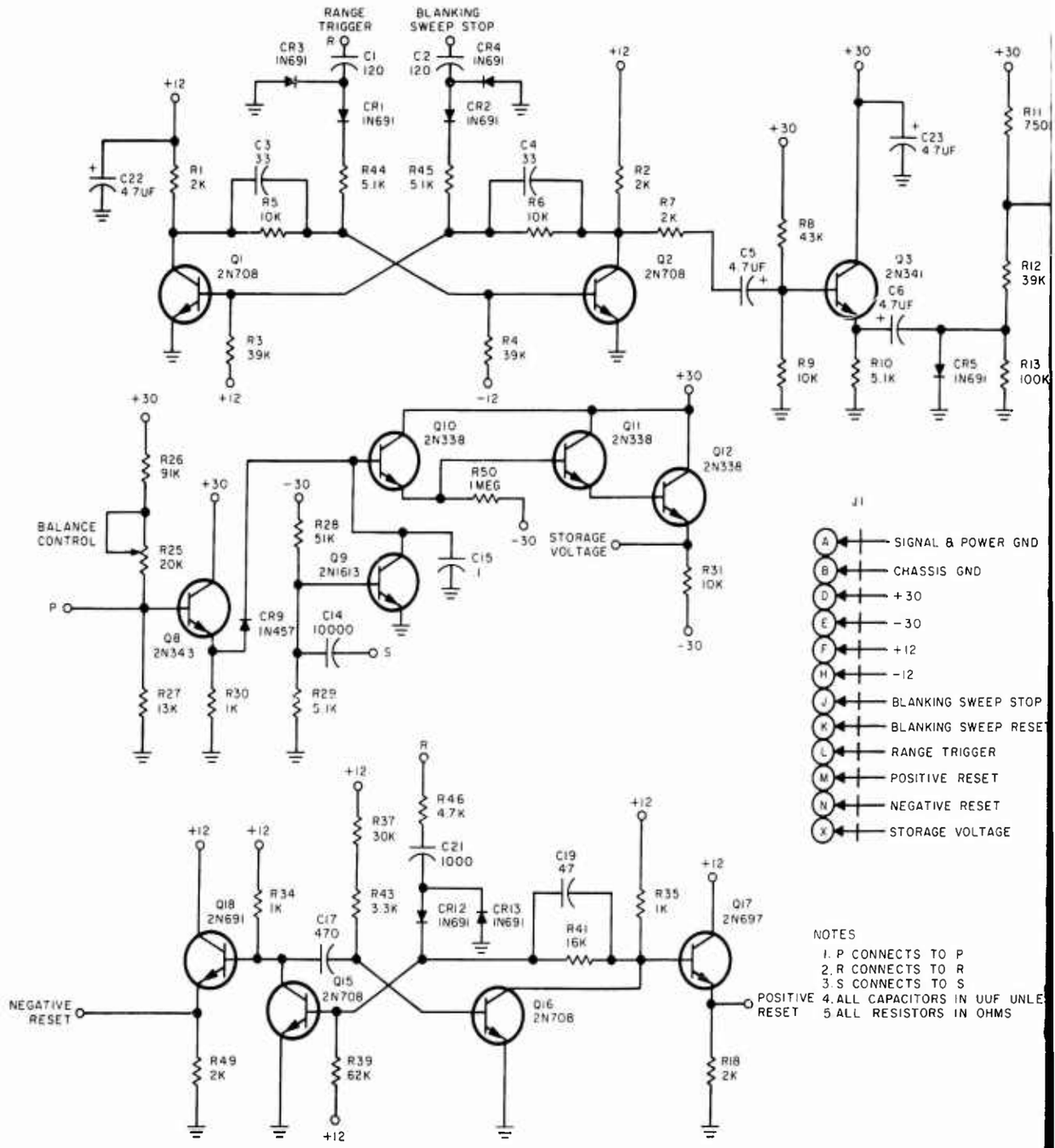


NOTES.
1. CONNECT A-A'
2. ALL RESISTORS IN OHMS
3. ALL CAPACITORS IN PF
4. ALL DIODES TYPE IN691
5. ALL TRANSISTORS TYPE 2N708
6. COMPONENT SERIES DESIGNATION IS 2600

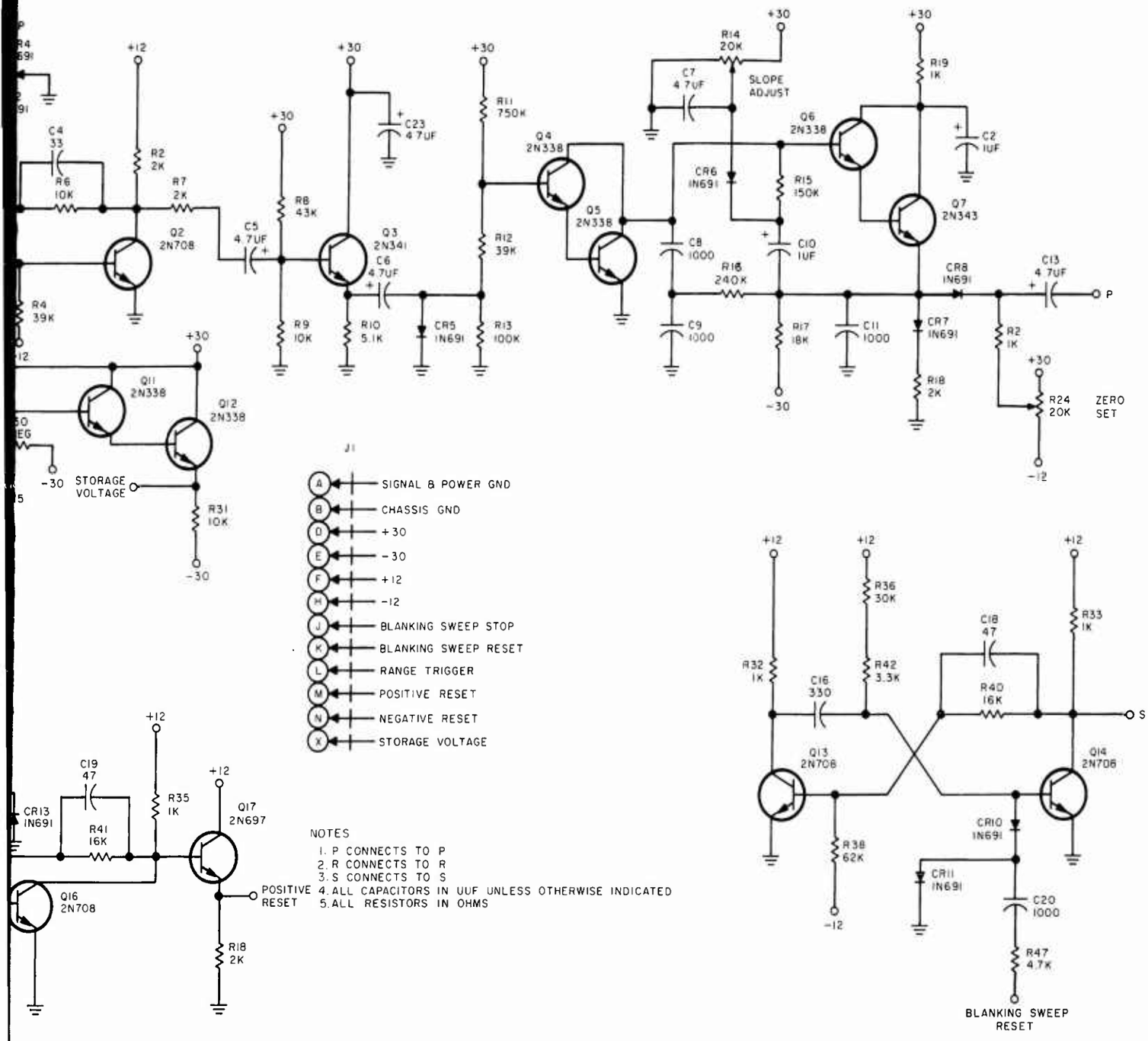
2

FIGURE 5-24

BLANKING LOGIC (2600)


RANGE TRIGGER
BLANKING SWEEP STOP
CR3 IN691
C1 120
C2 120
CR4 IN691
CR1 IN691
CR2 IN691
+12
+30
C22 4.7UF
R1 2K
C3 33
R5 10K
R44 5.1K
R45 5.1K
C4 33
R6 10K
R2 2K
R7 2K
C23 4.7UF
R11 750
R8 43K
C5 4.7UF
Q1 2N708
Q2 2N708
Q3 2N341
C6 4.7UF
R12 39K
R3 39K
R4 39K
R9 10K
R10 5.1K
CR5 IN691
R13 100K
-12
Q10 2N338
Q11 2N338
Q12 2N338
R50 1MEG
-30
R26 91K
R28 51K
C15 1
STORAGE VOLTAGE
R31 10K
BALANCE CONTROL
R25 20K
Q9 2N1613
P
CR9 IN457
C14 10000
S
Q8 2N343
R27 13K
R30 1K
R29 5.1K
J1
A SIGNAL & POWER GND
B CHASSIS GND
D +30
E -30
F +12
H -12
J BLANKING SWEEP STOP
K BLANKING SWEEP RESET
L RANGE TRIGGER
M POSITIVE RESET
N NEGATIVE RESET
X STORAGE VOLTAGE
R
R46 4.7K
R37 30K
C21 1000
C19 47
R34 1K
R43 3.3K
CR12 IN691
CR13 IN691
R41 16K
R35 1K
Q17 2N697
Q18 2N691
C17 470
Q15 2N708
Q16 2N708
NEGATIVE RESET
POSITIVE RESET
R49 2K
R39 62K
R18 2K
NOTES
1. P CONNECTS TO P
2. R CONNECTS TO R
3. S CONNECTS TO S
4. ALL CAPACITORS IN UUF UNLE
5 ALL RESISTORS IN OHMS

1

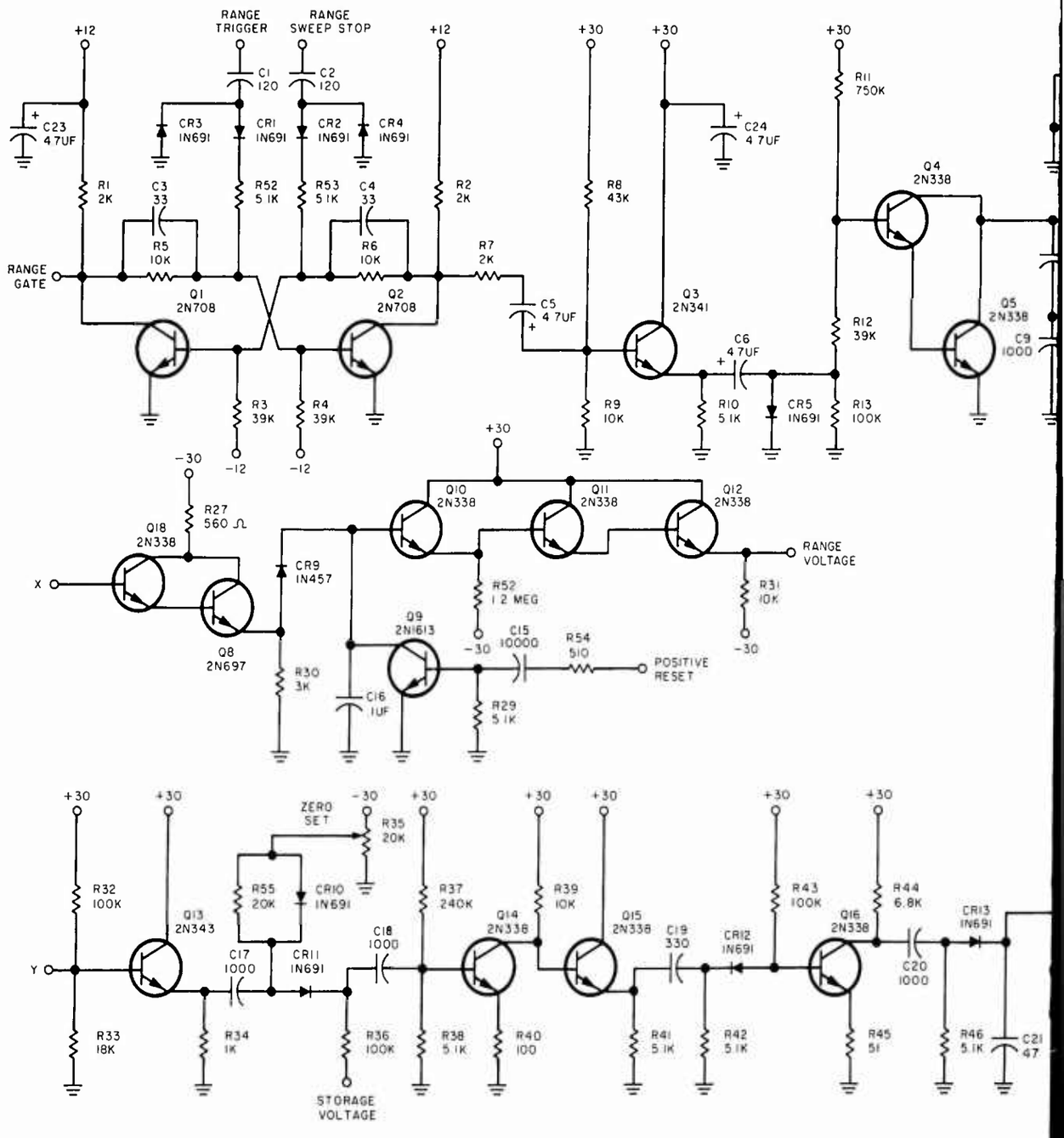


NOTES

1. P CONNECTS TO P
2. R CONNECTS TO R
3. S CONNECTS TO S
4. ALL CAPACITORS IN UUF UNLESS OTHERWISE INDICATED
5. ALL RESISTORS IN OHMS

FIGURE 5-25

BLANKING SWEEP GENERATOR (2700)


RANGE TRIGGER
RANGE SWEEP STOP
+12
+30
C1 120
C2 120
C23 4.7UF
C24 4.7UF
CR3 IN691
CR1 IN691
CR2 IN691
CR4 IN691
R1 2K
C3 33
R52 5.1K
R53 5.1K
C4 33
R2 2K
R8 43K
R11 750K
Q4 2N338
R5 10K
R6 10K
R7 2K
RANGE GATE
Q1 2N708
Q2 2N708
C5 4.7UF
Q3 2N341
C6 4.7UF
Q5 2N338
C9 1000
R12 39K
R3 39K
R4 39K
R9 10K
R10 5.1K
CR5 IN691
R13 100K
-30
-12
R27 560 Ω
Q10 2N338
Q11 2N338
Q12 2N338
Q18 2N338
RANGE VOLTAGE
X
CR9 IN457
R52 1.2 MEG
R31 10K
Q9 2N1613
C15 10000
R54 510
POSITIVE RESET
Q8 2N697
R30 3K
C16 1UF
R29 5.1K
ZERO SET
R35 20K
R32 100K
R55 20K
CR10 IN691
R37 240K
R39 10K
R43 100K
R44 6.8K
CR13 IN691
Q13 2N343
C18 1000
Q14 2N338
Q15 2N338
C19 330
CR12 IN691
Q16 2N338
Y
C17 1000
CR11 IN691
C20 1000
R33 18K
R34 1K
R36 100K
R38 5.1K
R40 100
R41 5.1K
R42 5.1K
R45 51
R46 5.1K
C21 47
STORAGE VOLTAGE

1

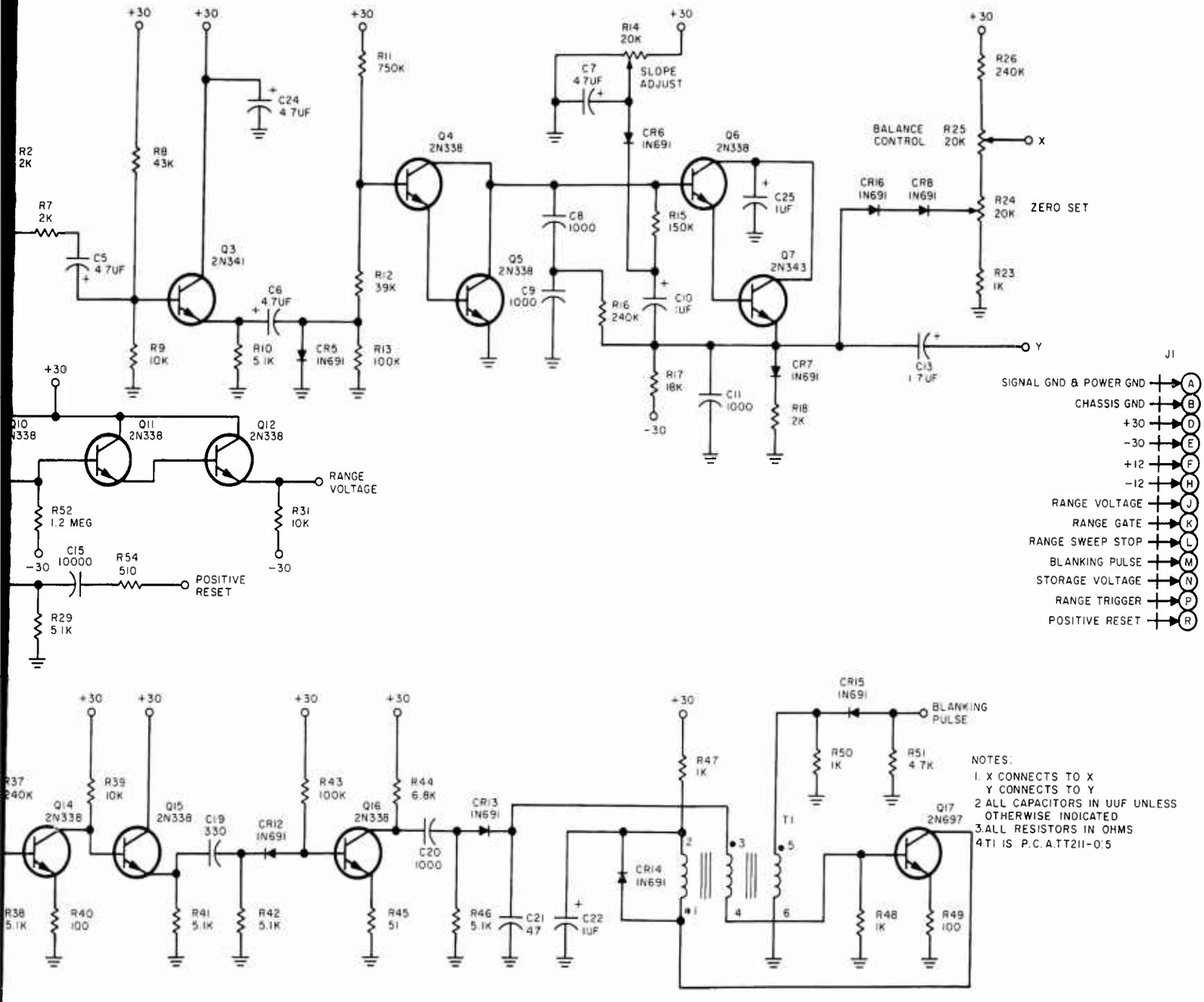


FIGURE 5-26

RANGE SWEEP GENERATOR (2800)

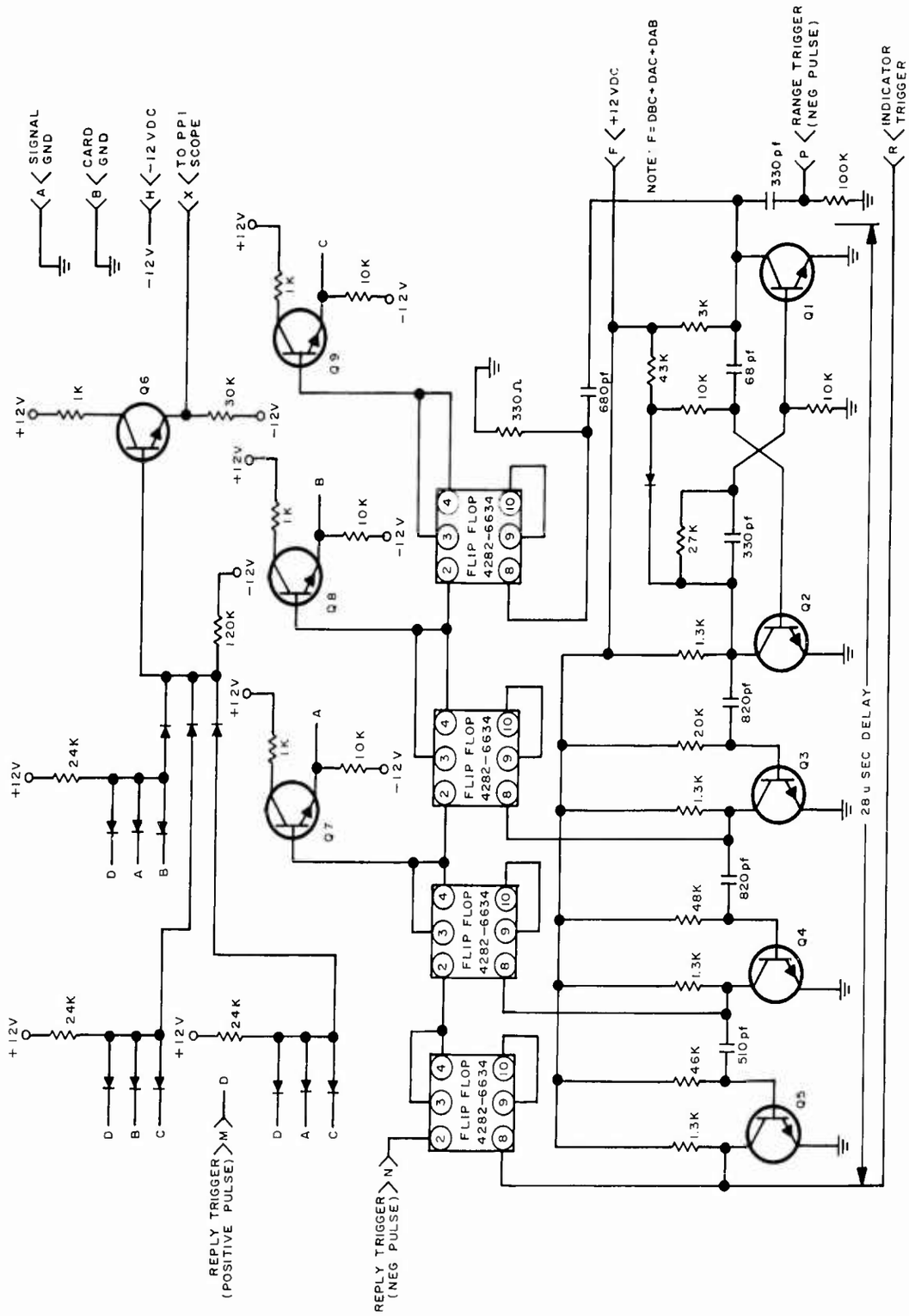
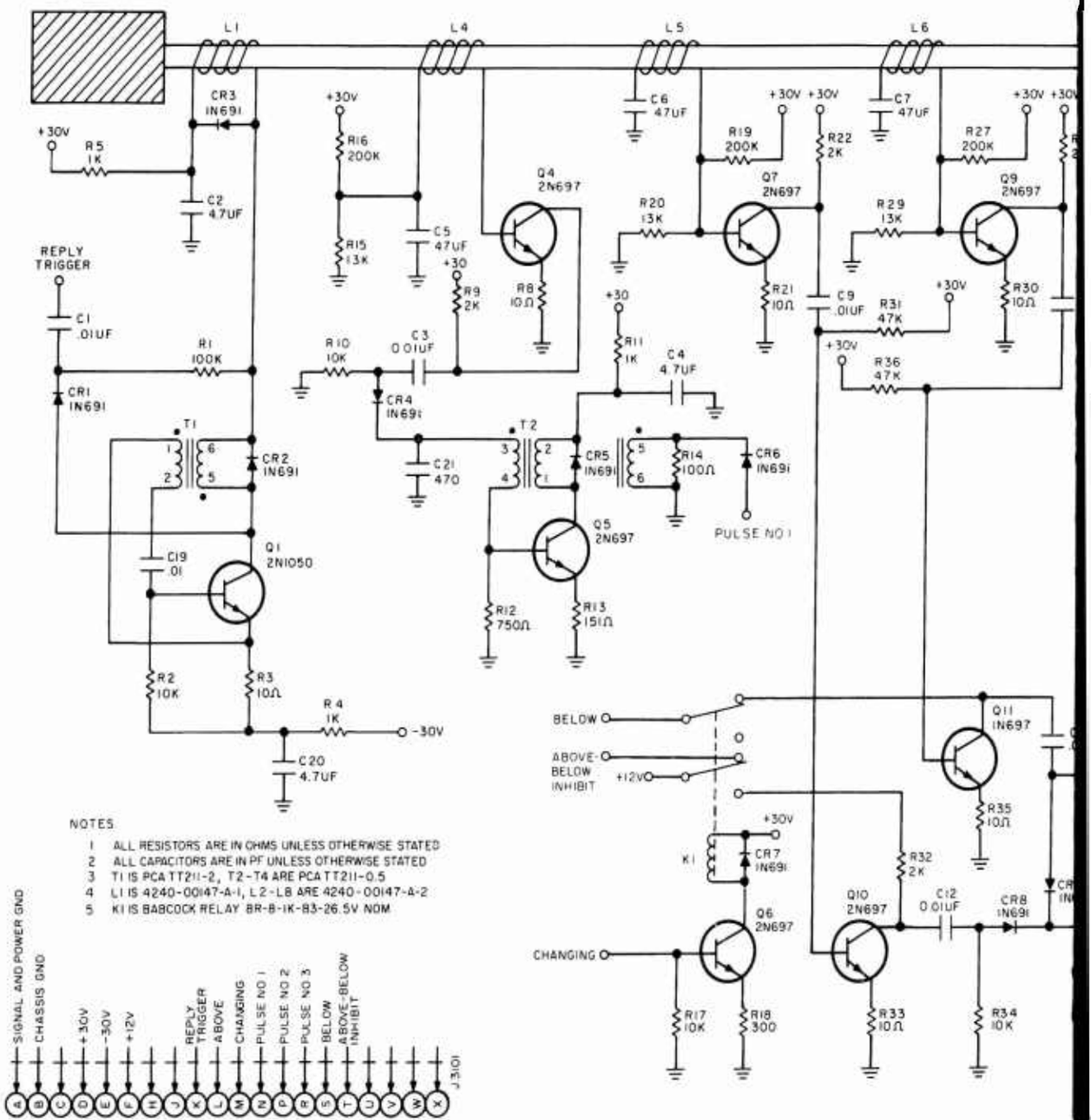
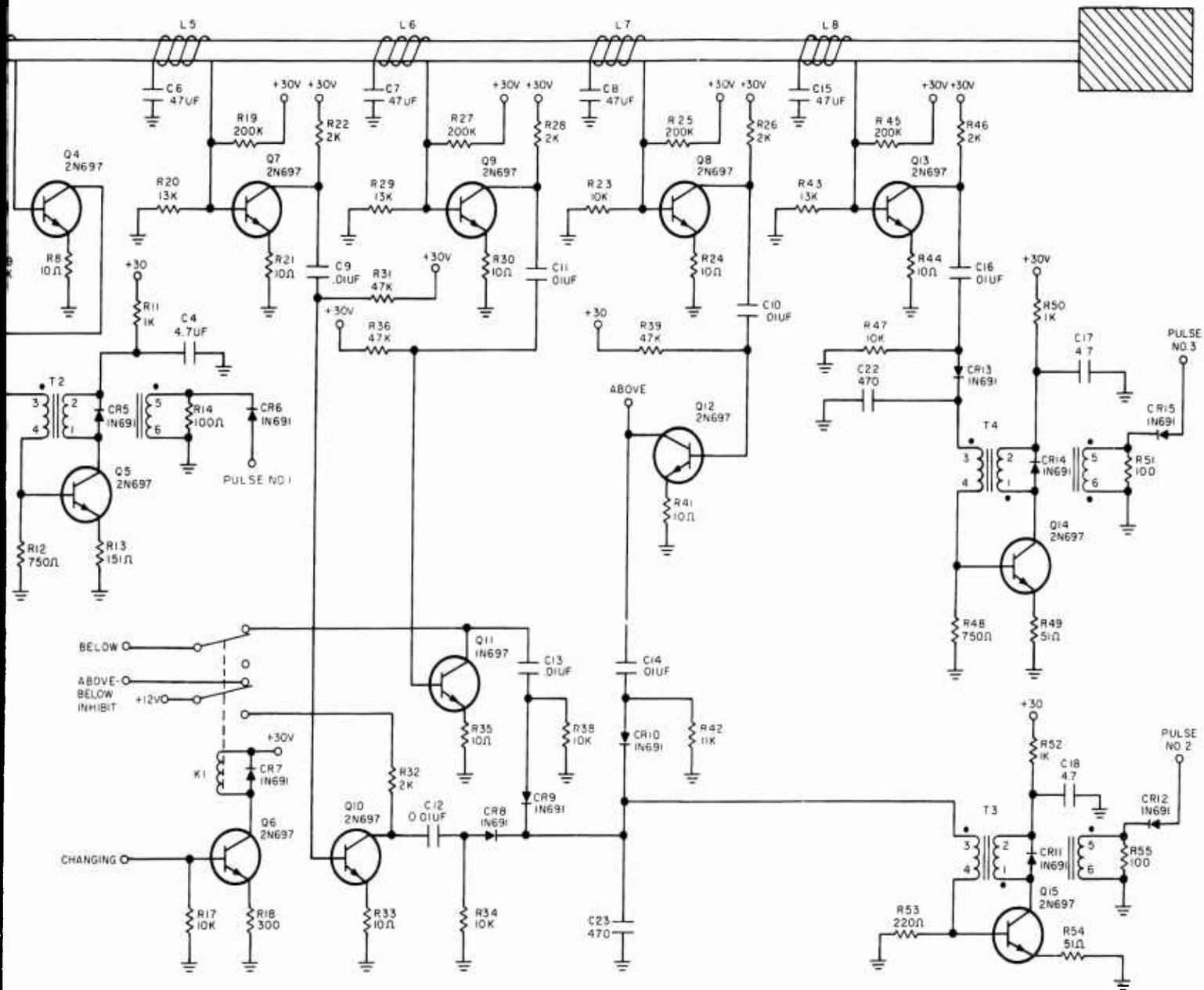


FIGURE 5 27. PWI DISPLAY LOGIC (2900)


L1
L4
L5
L6
CR3 IN691
+30V
R5 1K
C2 4.7UF
REPLY TRIGGER
C1 .01UF
R1 100K
CR1 IN691
T1
CR2 IN691
C19 .01
Q1 2N1050
R2 10K
R3 10Ω
R4 1K
-30V
C20 4.7UF
R16 200K
R15 13K
C5 47UF
+30
R9 2K
Q4 2N697
R8 10Ω
R10 10K
C3 0.01UF
CR4 IN691
C21 470
T2
R11 1K
C4 4.7UF
CR5 IN691
R14 100Ω
CR6 IN691
PULSE NO 1
Q5 2N697
R12 750Ω
R13 151Ω
C6 47UF
R19 200K
R22 2K
Q7 2N697
R20 13K
R21 10Ω
C7 47UF
R27 200K
Q9 2N697
R29 13K
R30 10Ω
C9 .01UF
R31 47K
R36 47K
BELOW
ABOVE-BELOW INHIBIT
+12V
Q11 IN697
R35 10Ω
K1
CR7 IN691
R32 2K
Q6 2N697
Q10 2N697
C12 0.01UF
CR8 IN691
CHANGING
R17 10K
R18 300
R33 10Ω
R34 10K
NOTES
1 ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE STATED
2 ALL CAPACITORS ARE IN PF UNLESS OTHERWISE STATED
3 T1 IS PCA TT211-2, T2-T4 ARE PCA TT211-0.5
4 L1 IS 4240-00147-A-1, L2-L8 ARE 4240-00147-A-2
5 K1 IS BABCOCK RELAY BR-8-1K-83-26.5V NOM
SIGNAL AND POWER GND
CHASSIS GND
+30V
-30V
+12V
REPLY TRIGGER
ABOVE
CHANGING
PULSE NO 1
PULSE NO 2
PULSE NO 3
BELOW
ABOVE-BELOW INHIBIT
J3101

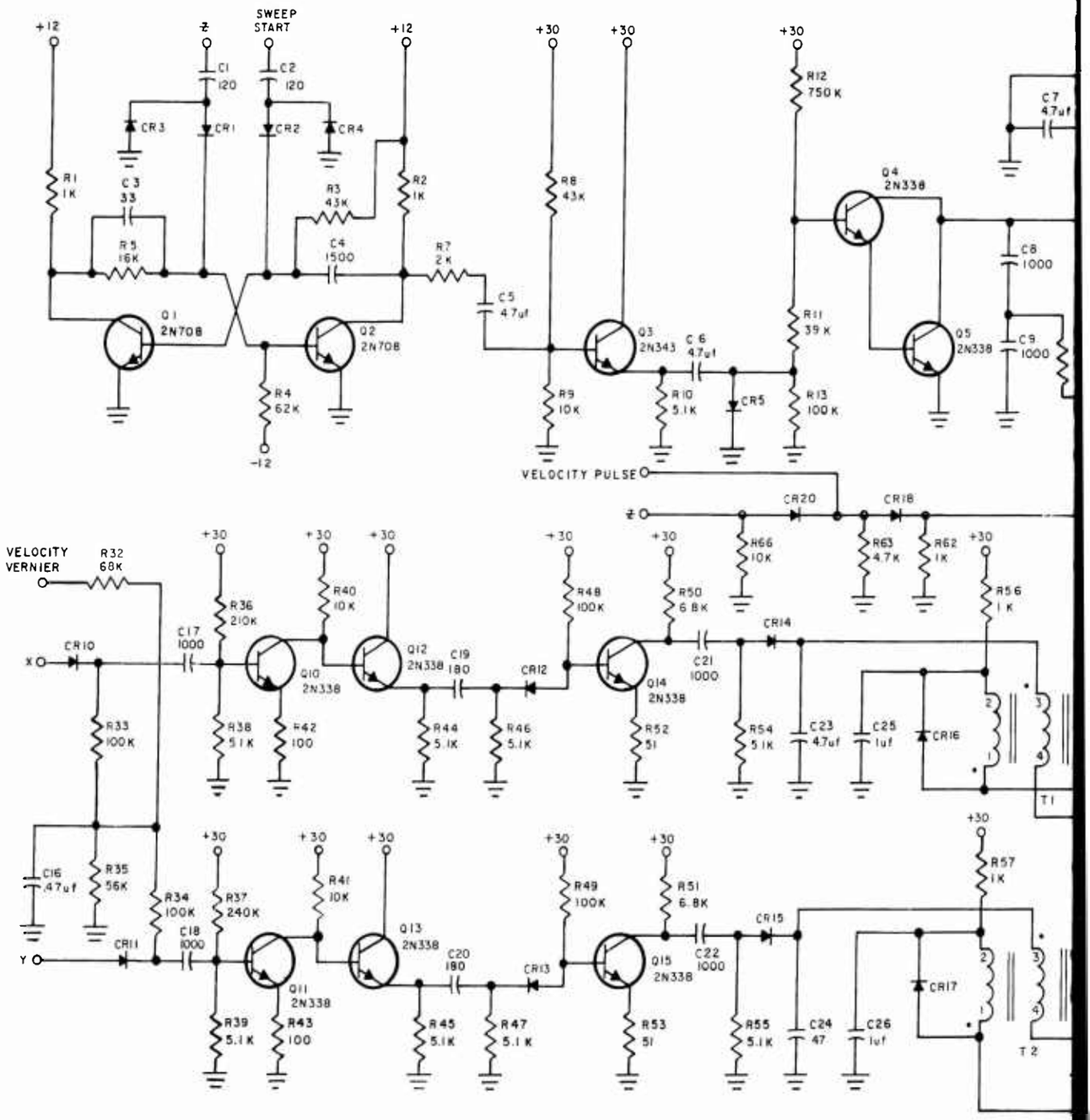
1



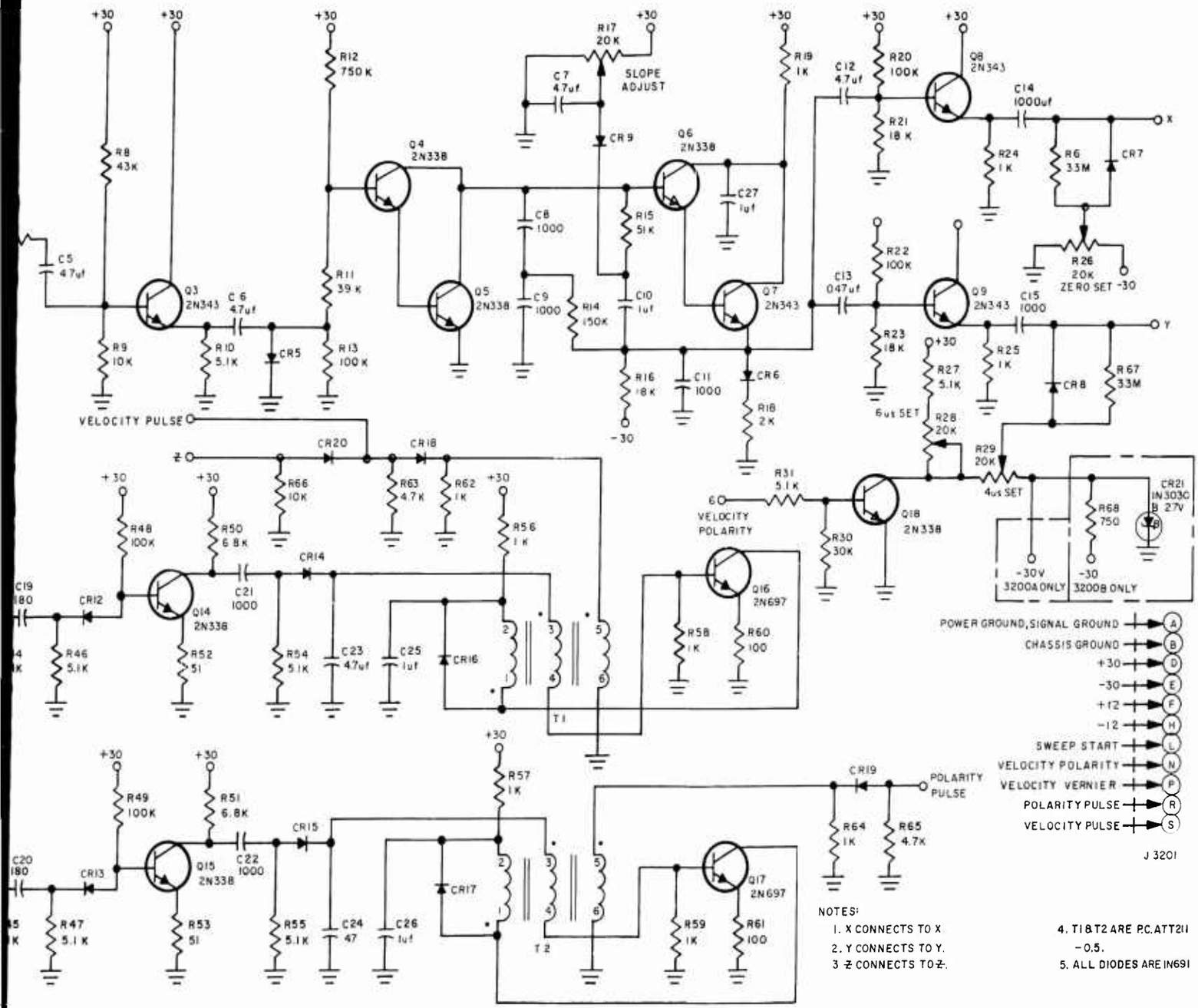
2

FIGURE 5-28

TRANSPONDER ENCODER DELAY SELECTOR (3100)


+12
-Z
SWEEP START
+12
+30
+30
+30
R1 1K
C1 120
C2 120
CR3
CR1
CR2
CR4
C3 33
R3 43K
R2 1K
R5 16K
C4 1500
R7 2K
C5 4.7uf
R8 43K
R12 750K
C7 4.7uf
Q4 2N338
C8 1000
Q1 2N708
Q2 2N708
Q3 2N343
C6 47uf
R11 39K
Q5 2N338
C9 1000
R4 62K
-12
R9 10K
R10 5.1K
CR5
R13 100K
VELOCITY PULSE
-Z
CR20
CR18
VELOCITY VERNIER
R32 68K
+30
+30
+30
+30
+30
+30
+30
R66 10K
R63 4.7K
R62 1K
R56 1K
R36 210K
R40 10K
R48 100K
R50 6.8K
CR14
CR10
X
C17 1000
Q10 2N338
Q12 2N338
C19 180
CR12
Q14 2N338
C21 1000
R33 100K
R38 5.1K
R42 100
R44 5.1K
R46 5.1K
R52 51
R54 5.1K
C23 4.7uf
C25 1uf
CR16
T1
+30
+30
+30
+30
+30
+30
+30
R57 1K
C16 .47uf
R35 56K
R34 100K
R37 240K
R41 10K
R49 100K
R51 6.8K
CR15
CR11
Y
C18 1000
Q11 2N338
Q13 2N338
C20 180
CR13
Q15 2N338
C22 1000
CR17
R39 5.1K
R43 100
R45 5.1K
R47 5.1K
R53 51
R55 5.1K
C24 47
C26 1uf
T2

1

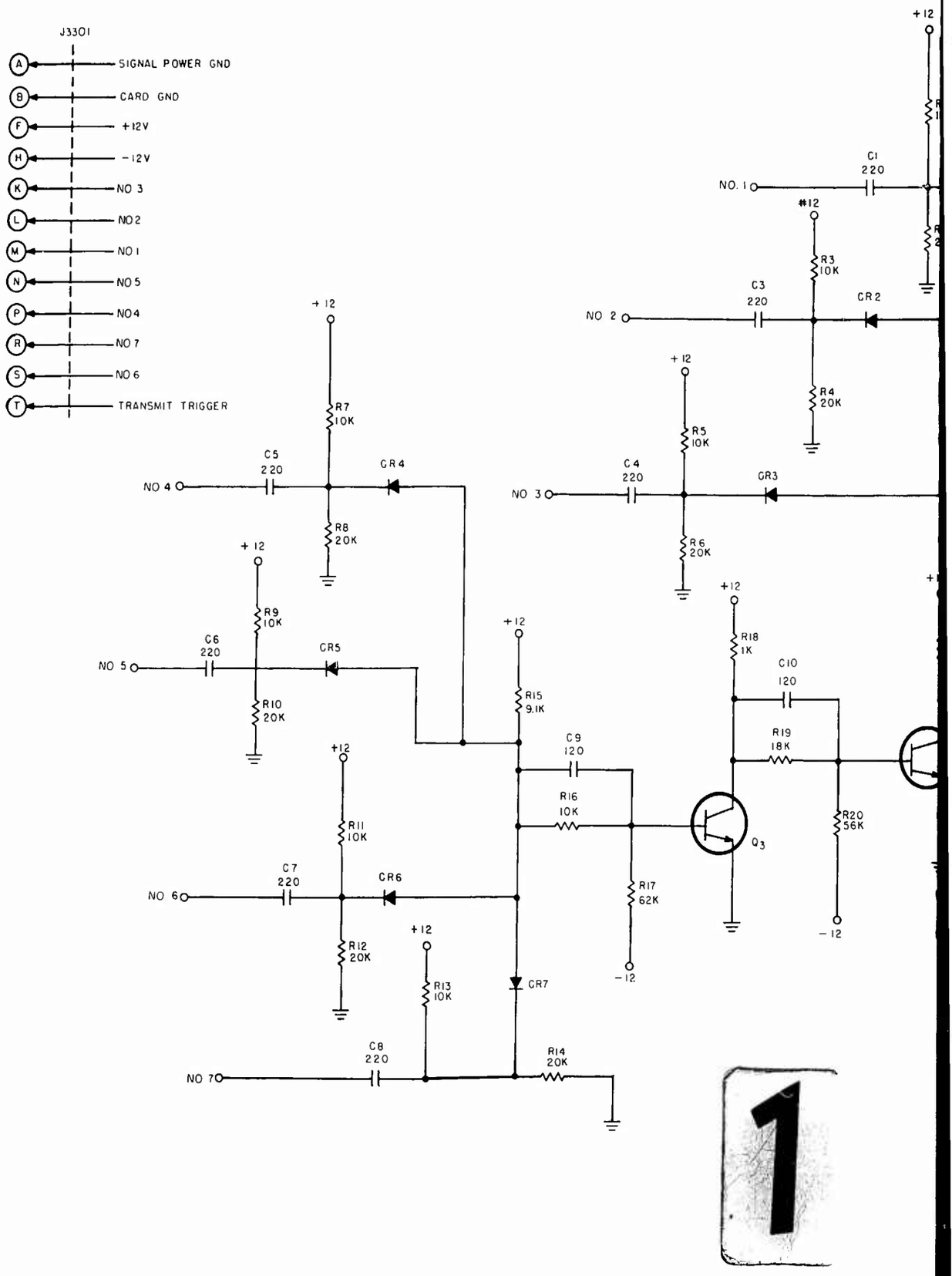


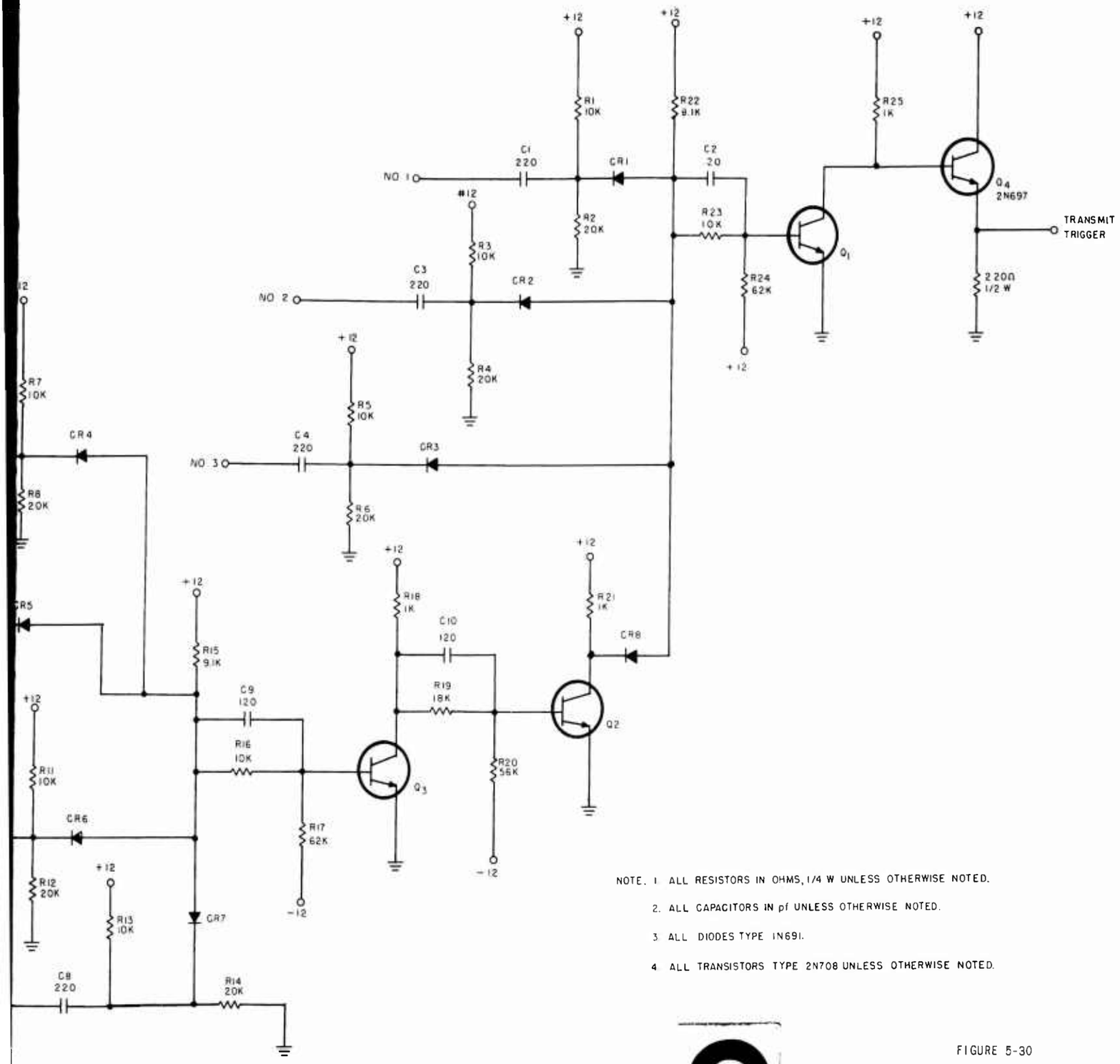
NOTES:

1. X CONNECTS TO X
2. Y CONNECTS TO Y.
3. Z CONNECTS TO Z.
4. T1 & T2 ARE P.C. ATT211 - 0.5.
5. ALL DIODES ARE IN691

FIGURE 5-29

NORTH-EAST VELOCITY CODER (3200)


J3301
A
SIGNAL POWER GND
B
CARD GND
F
+12V
H
-12V
K
NO 3
L
NO 2
M
NO 1
N
NO 5
P
NO 4
R
NO 7
S
NO 6
T
TRANSMIT TRIGGER
+12
C1
220
NO. 1
#12
R3
10K
C3
220
CR2
NO 2
R4
20K
R5
10K
C4
220
CR3
NO 3
R6
20K
R7
10K
C5
220
CR4
NO 4
R8
20K
R9
10K
C6
220
CR5
NO 5
R10
20K
R15
9.1K
R18
1K
C10
120
C9
120
R19
18K
R16
10K
Q3
R20
56K
-12
R11
10K
C7
220
CR6
NO 6
R17
62K
R12
20K
R13
10K
CR7
C8
220
NO 7
R14
20K



NOTE. 1. ALL RESISTORS IN OHMS, 1/4 W UNLESS OTHERWISE NOTED.

2. ALL CAPACITORS IN pf UNLESS OTHERWISE NOTED.

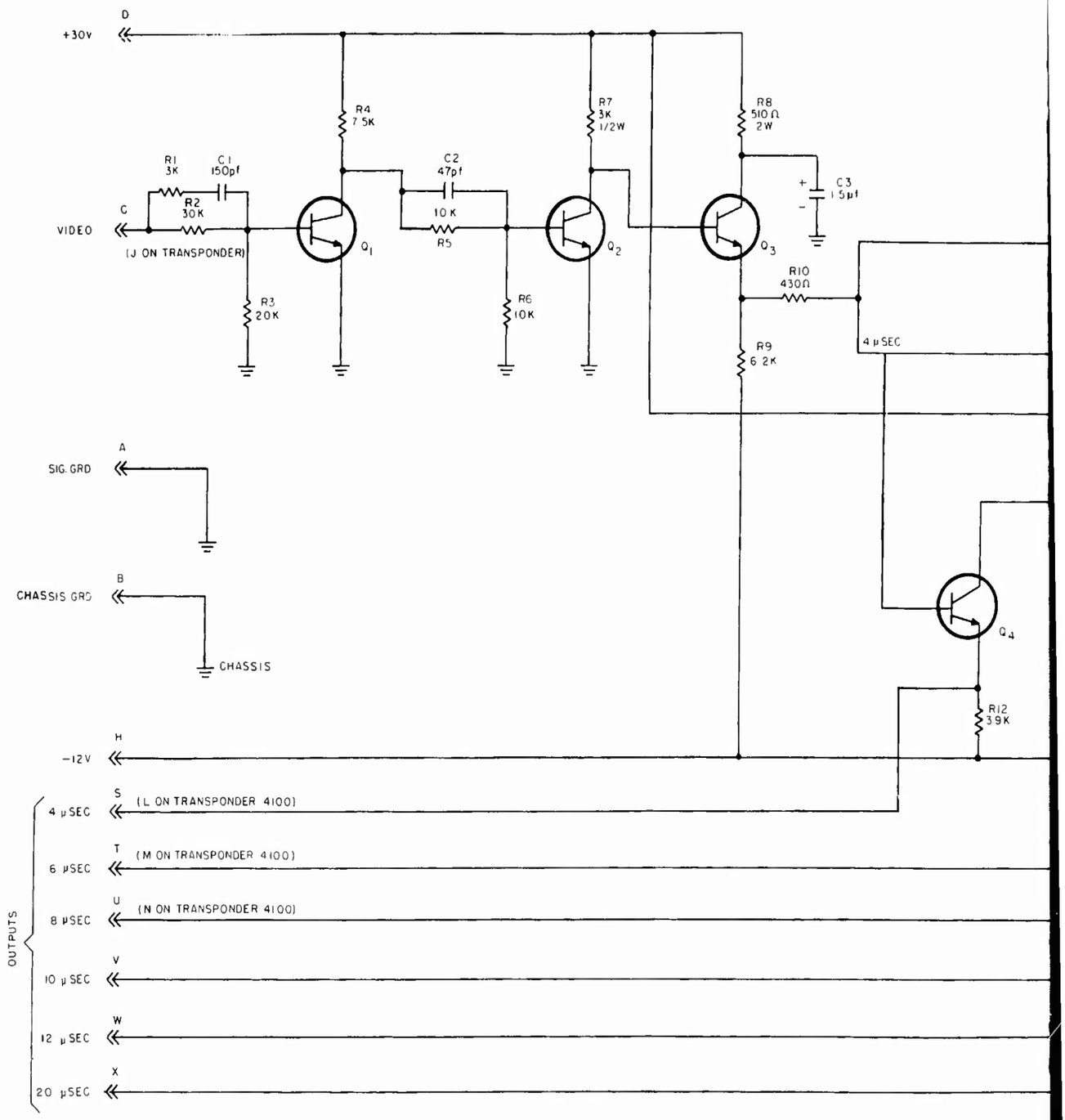
3. ALL DIODES TYPE 1N691.

4. ALL TRANSISTORS TYPE 2N708 UNLESS OTHERWISE NOTED.

2

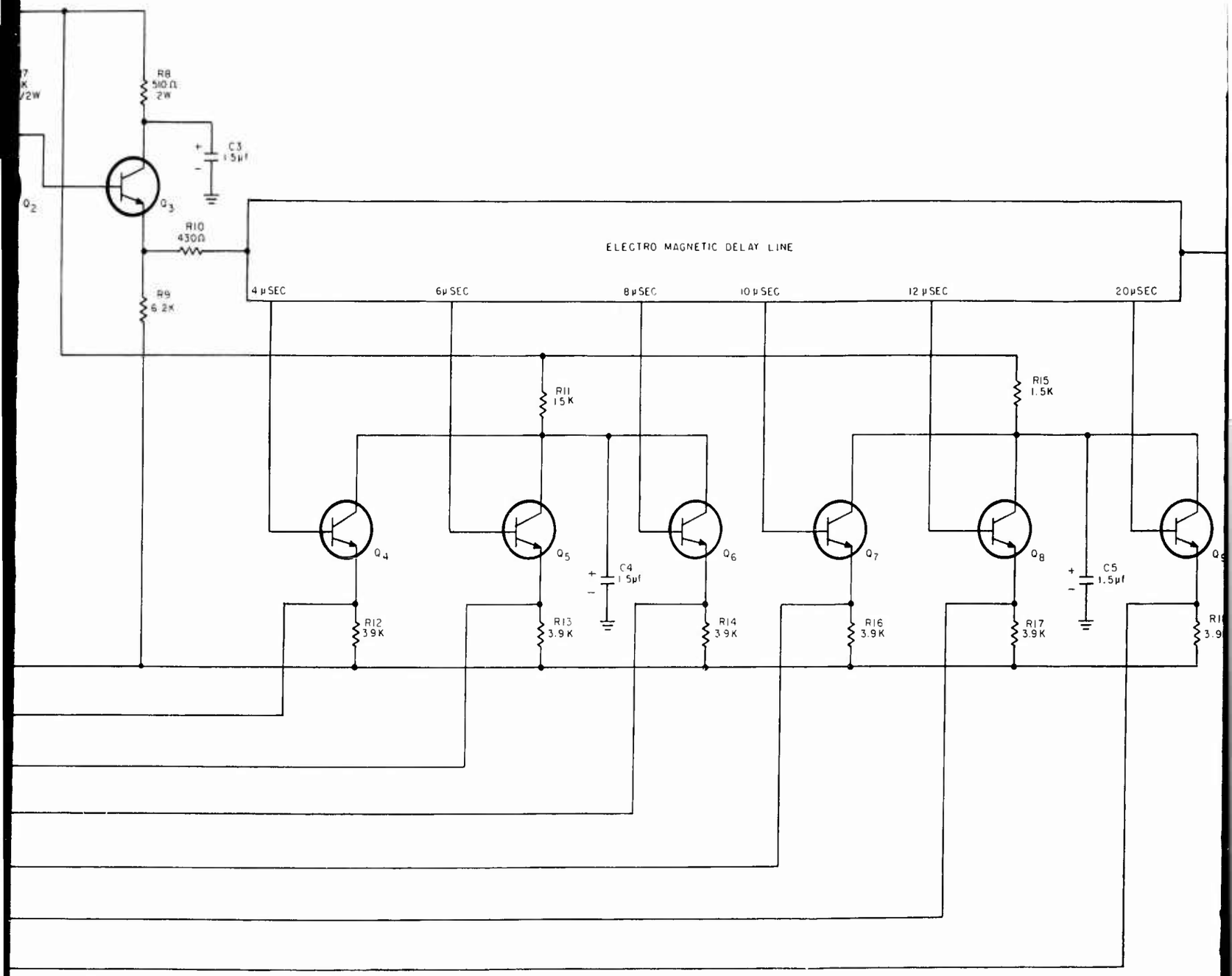
FIGURE 5-30

MIXER AMPLIFIER 3300 CAS SCHEMATIC



NOTE Q_7, Q_8, & Q_9, AND OUTPUTS (10 μSEC, 12 μSEC, 20 μSEC) DO NOT EXIST ON TRANSPONDER DECODER DELAY LINE

1



μSEC, 20 μSEC) DO NOT EXIST ON TRANSPONDER DECODER DELAY LINE CHASSIS 4100.

Q_1 Q_4 — — — Q_9 — — — — — 2N1104 OR 2N338

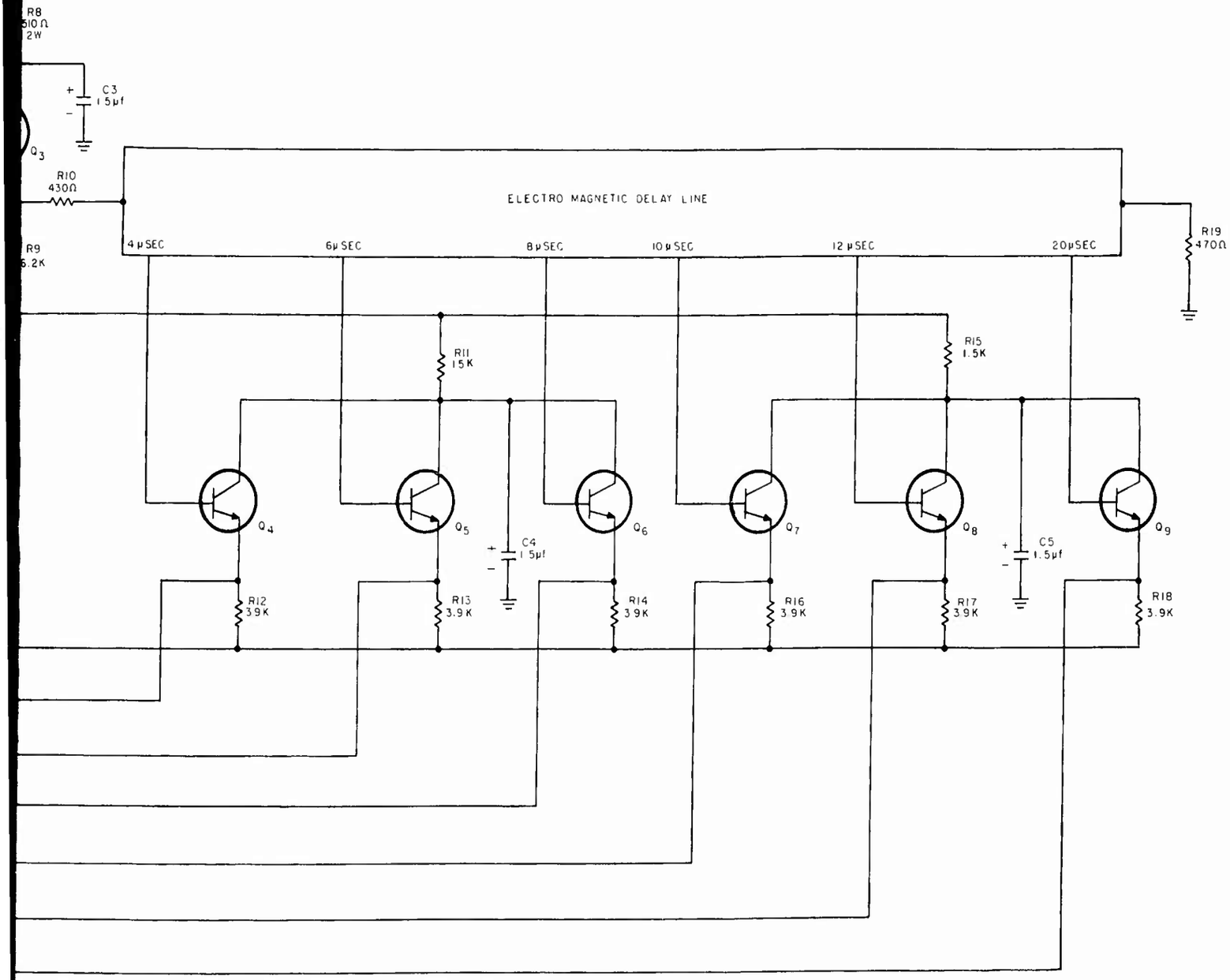
Q_2 — — — — — — — — — 2N708

Q_3 — — — — — — — — — 2N699

2

FIGURE 5-31

TRANSPONDER DECODER DELAY SELECTOR NO. 1



EXIST ON TRANSPONDER DECODER DELAY LINE CHASSIS 4100.

Q_1 Q_4 — — — Q_9 — — — — 2N1104 OR 2N338

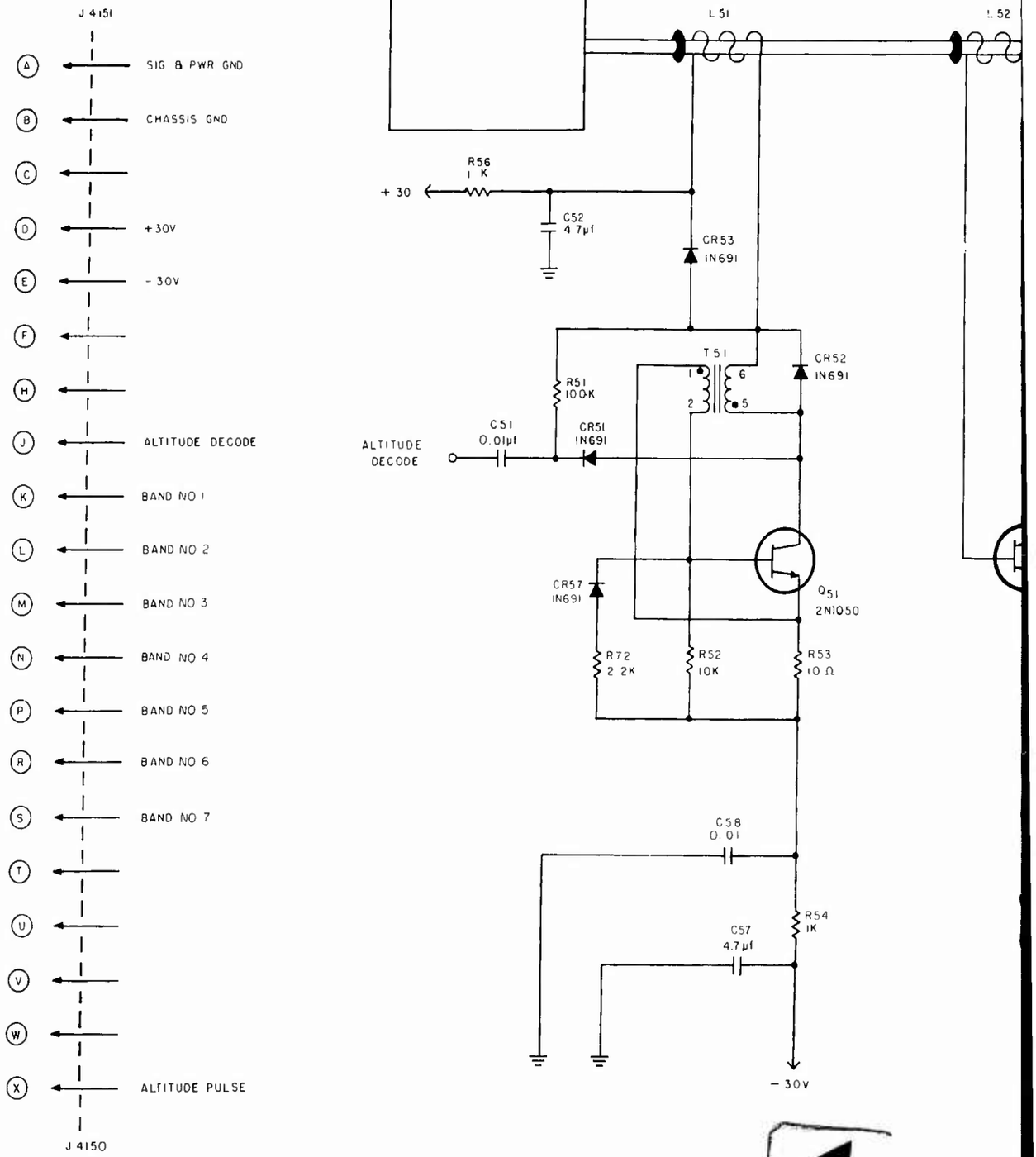
Q_2 — — — — — — — — 2N708

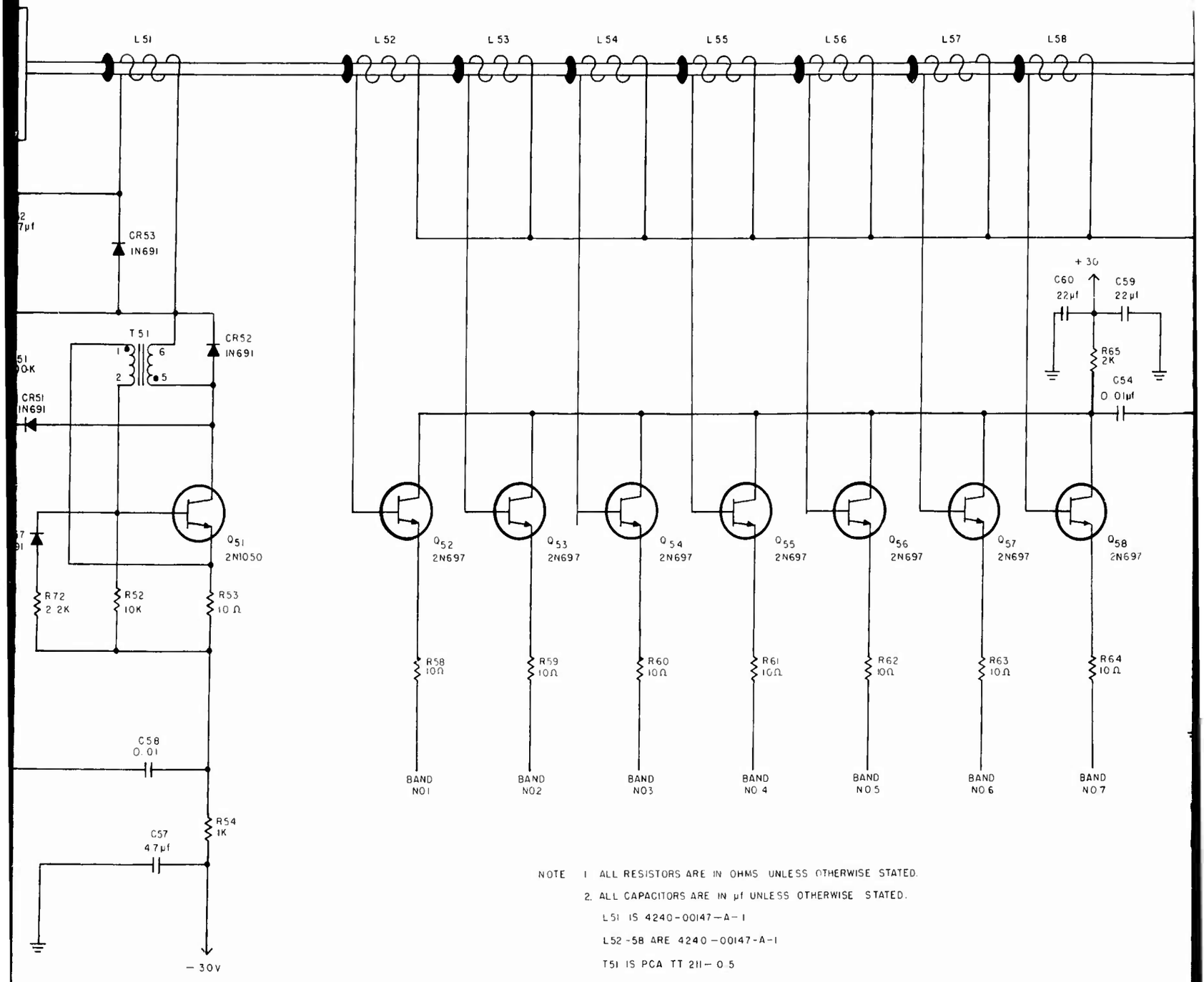
Q_3 — — — — — — — — 2N699

3

FIGURE 5-31

TRANSPONDER DECODER DELAY SELECTOR NO. 1 (4100)


J 4151
A
SIG & PWR GND
B
CHASSIS GND
C
D
+30V
E
- 30V
F
H
J
ALTITUDE DECODE
K
BAND NO 1
L
BAND NO 2
M
BAND NO 3
N
BAND NO 4
P
BAND NO 5
R
BAND NO 6
S
BAND NO 7
T
U
V
W
X
ALTITUDE PULSE
J 4150
L 51
L 52
R56
1 K
+ 30
C52
4.7µf
CR53
IN691
T 51
1
2
6
5
CR52
IN691
R51
100K
C51
0.01µf
CR51
IN691
ALTITUDE
DECODE
CR57
IN691
Q51
2N1050
R72
2.2K
R52
10K
R53
10 Ω
C58
0.01
R54
1K
C57
4.7µf
- 30V



NOTE 1. ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE STATED.

2. ALL CAPACITORS ARE IN μf UNLESS OTHERWISE STATED.

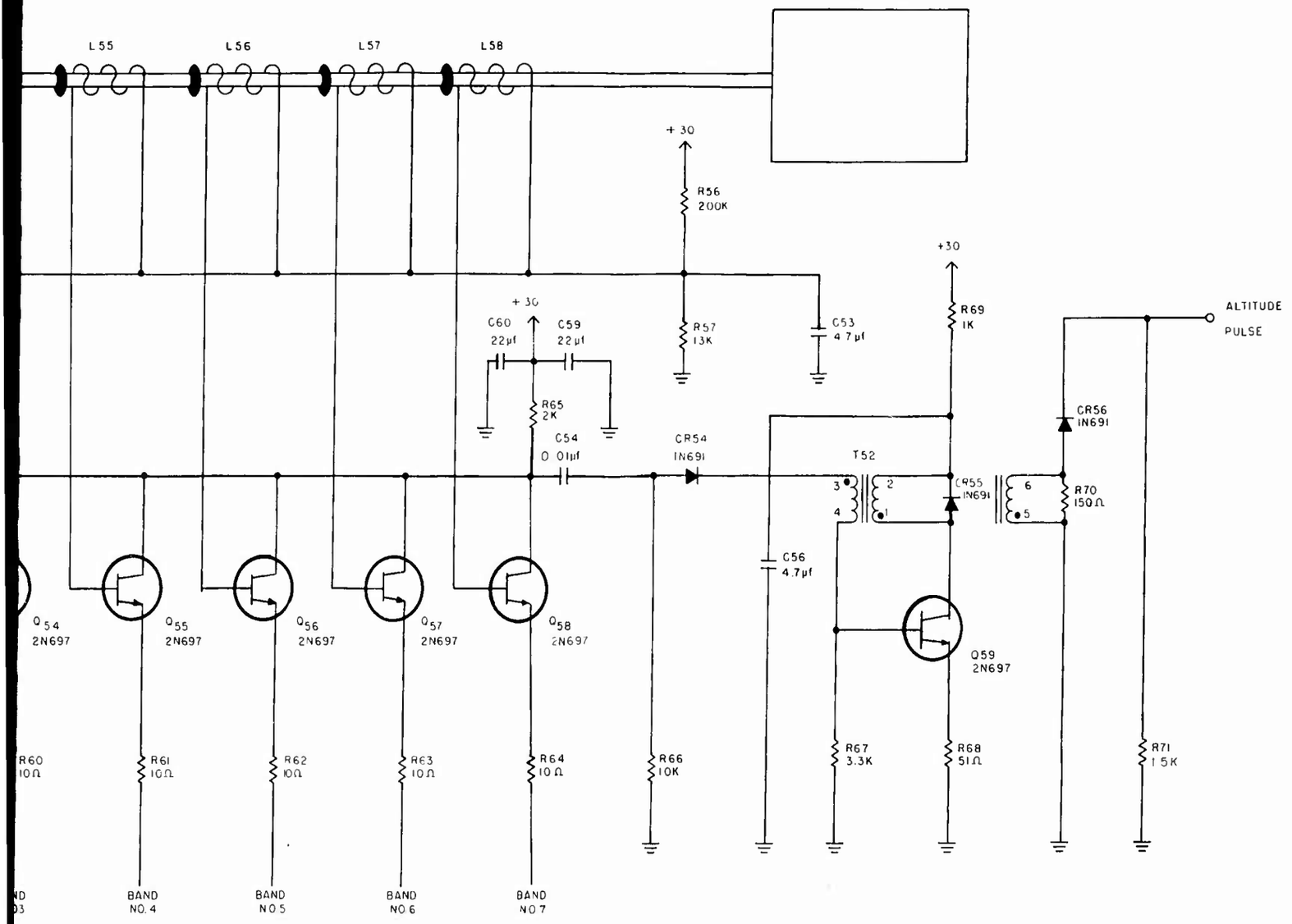
L51 IS 4240-00147-A-1

L52-58 ARE 4240-00147-A-1

T51 IS PCA TT 211-0.5

T52 IS PCA TT111-1

2



ISTORS ARE IN OHMS UNLESS OTHERWISE STATED.

ACITORS ARE IN μf UNLESS OTHERWISE STATED.

4240-00147-A-1

ARE 4240-00147-A-1

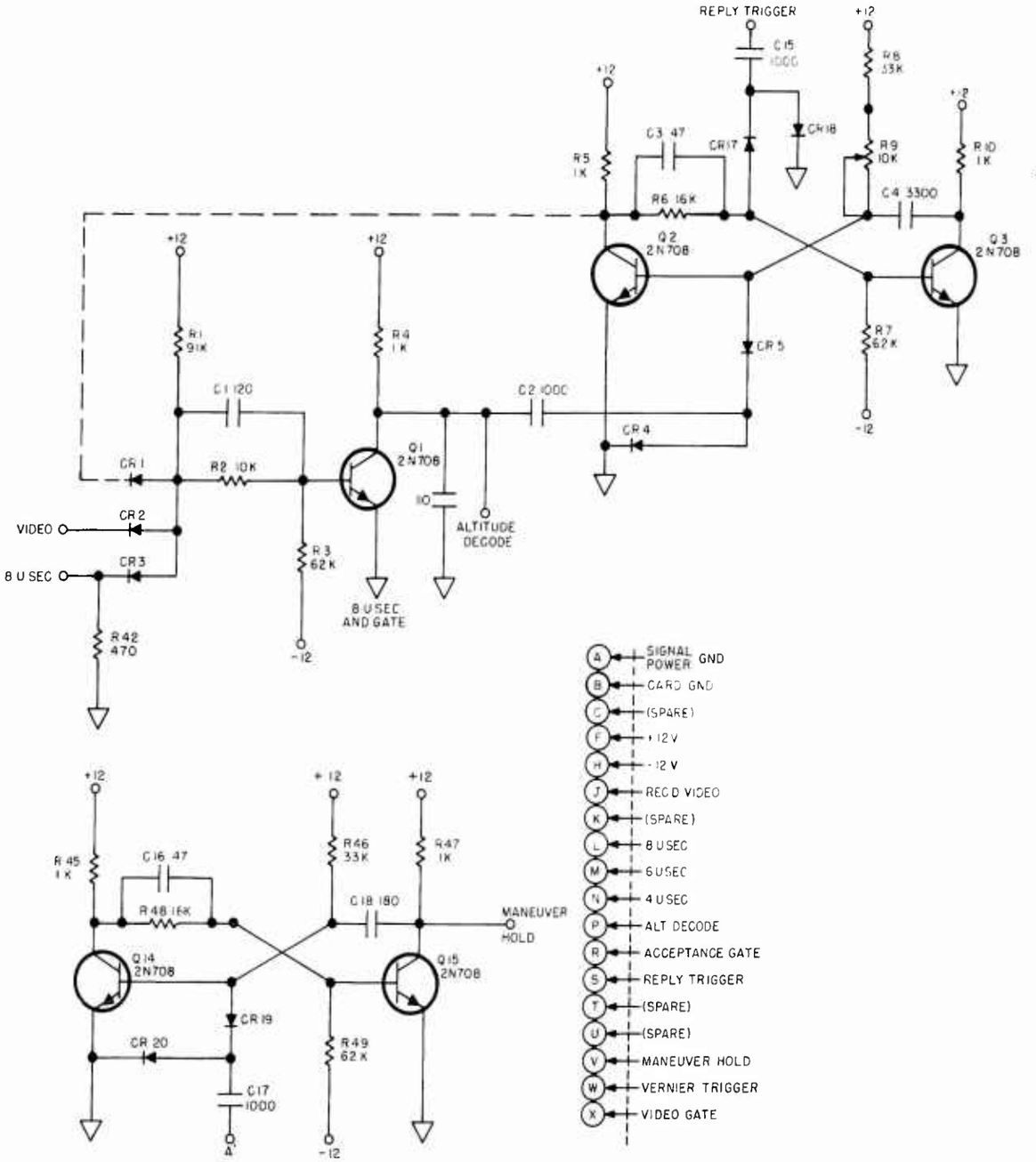
PCA TT 211-0.5

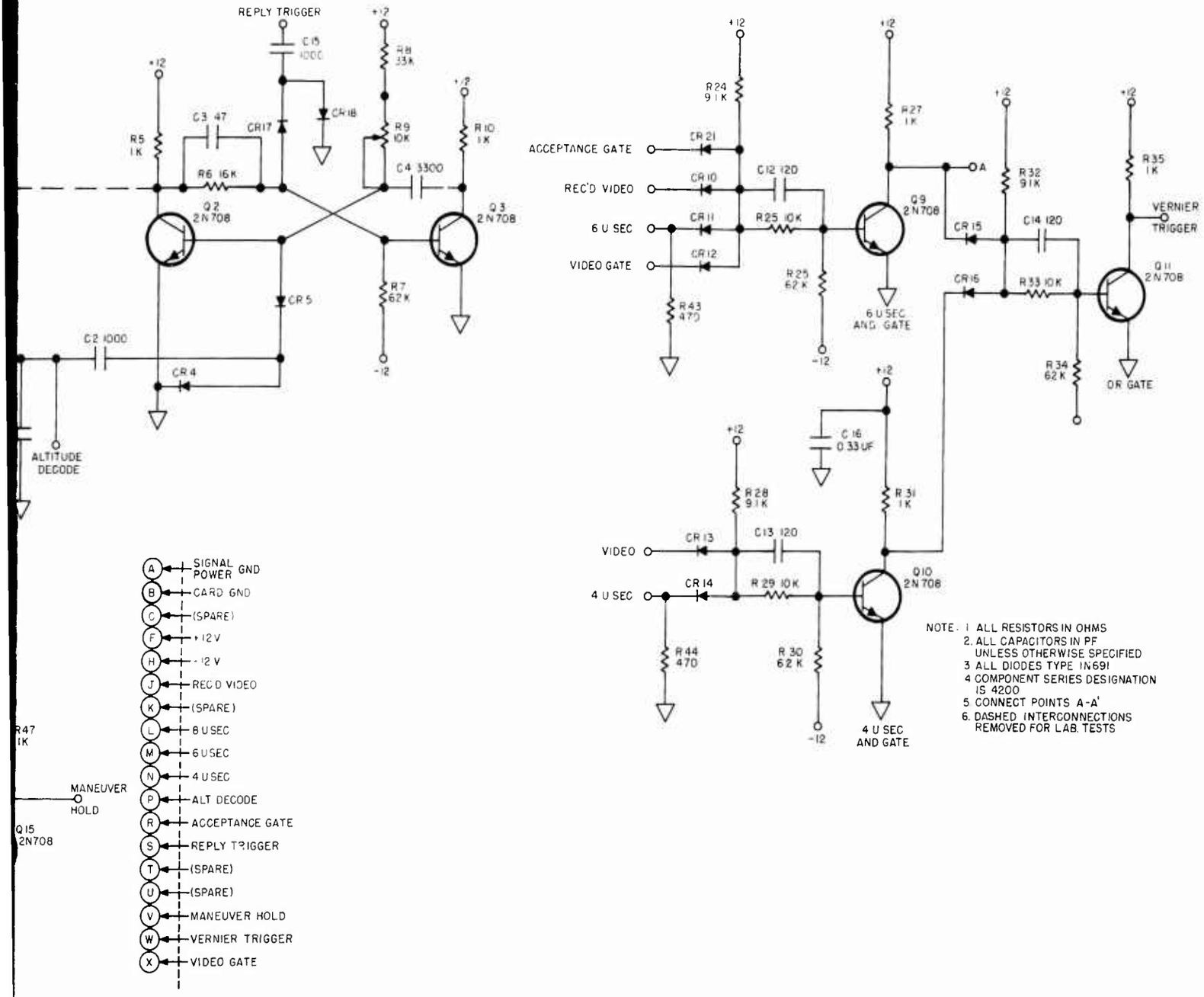
PCA TT111-1

3

FIGURE 5-32.

TRANSPONDER DECODER DELAY SELECTOR NO. 2 (4150)

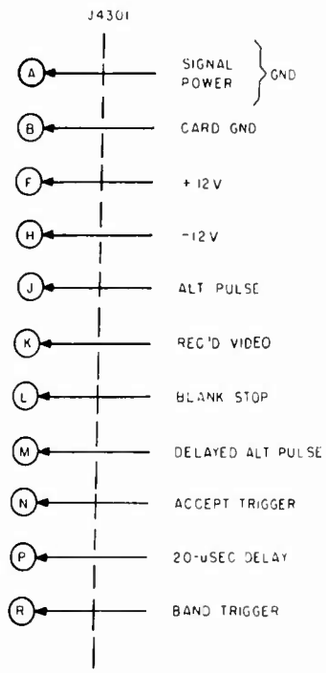

REPLY TRIGGER
+12
C15 1000
R8 33K
R5 1K
C3 47
CR17
CR18
R9 10K
R10 1K
R6 16K
C4 3300
Q2 2N708
Q3 2N708
R1 91K
R4 1K
CR5
R7 62K
C1 120
C2 1000
CR4
-12
CR1
R2 10K
Q1 2N706
110
ALTITUDE DECODE
VIDEO
CR2
8 U SEC
CR3
R3 62K
8 U SEC AND GATE
R42 470
R45 1K
C16 47
R46 33K
R47 1K
R48 16K
C18 180
MANEUVER HOLD
Q14 2N708
Q15 2N708
CR19
CR 20
R49 62K
C17 1000
A
SIGNAL POWER GND
CARD GND
(SPARE)
+12 V
-12 V
RECD VIDEO
(SPARE)
8 USEC
6 USEC
4 USEC
ALT DECODE
ACCEPTANCE GATE
REPLY TRIGGER
(SPARE)
(SPARE)
MANEUVER HOLD
VERNIER TRIGGER
VIDEO GATE



NOTE: 1. ALL RESISTORS IN OHMS
2. ALL CAPACITORS IN PF UNLESS OTHERWISE SPECIFIED
3. ALL DIODES TYPE IN691
4. COMPONENT SERIES DESIGNATION IS 4200
5. CONNECT POINTS A-A'
6. DASHED INTERCONNECTIONS REMOVED FOR LAB. TESTS

2

FIGURE 5-33
COMMAND DECODER (4200)



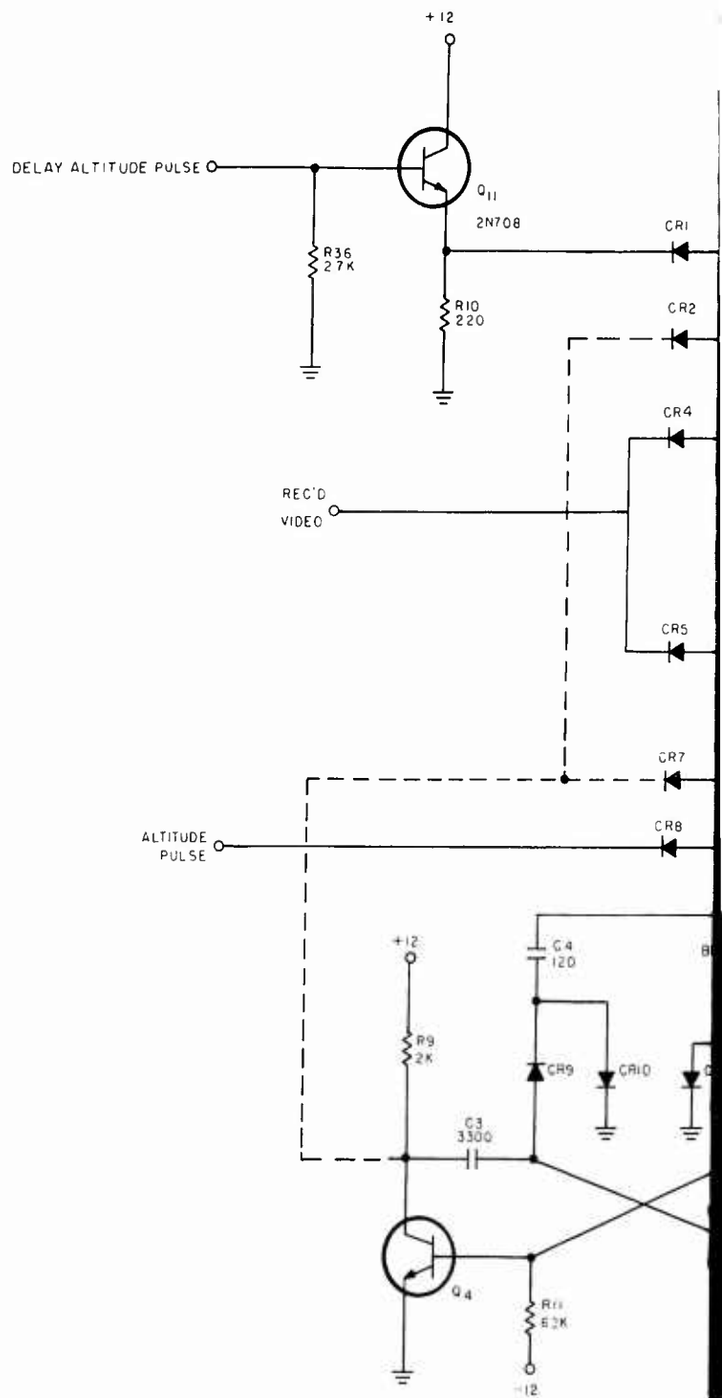
NOTE 1. ALL RESISTORS IN OHMS

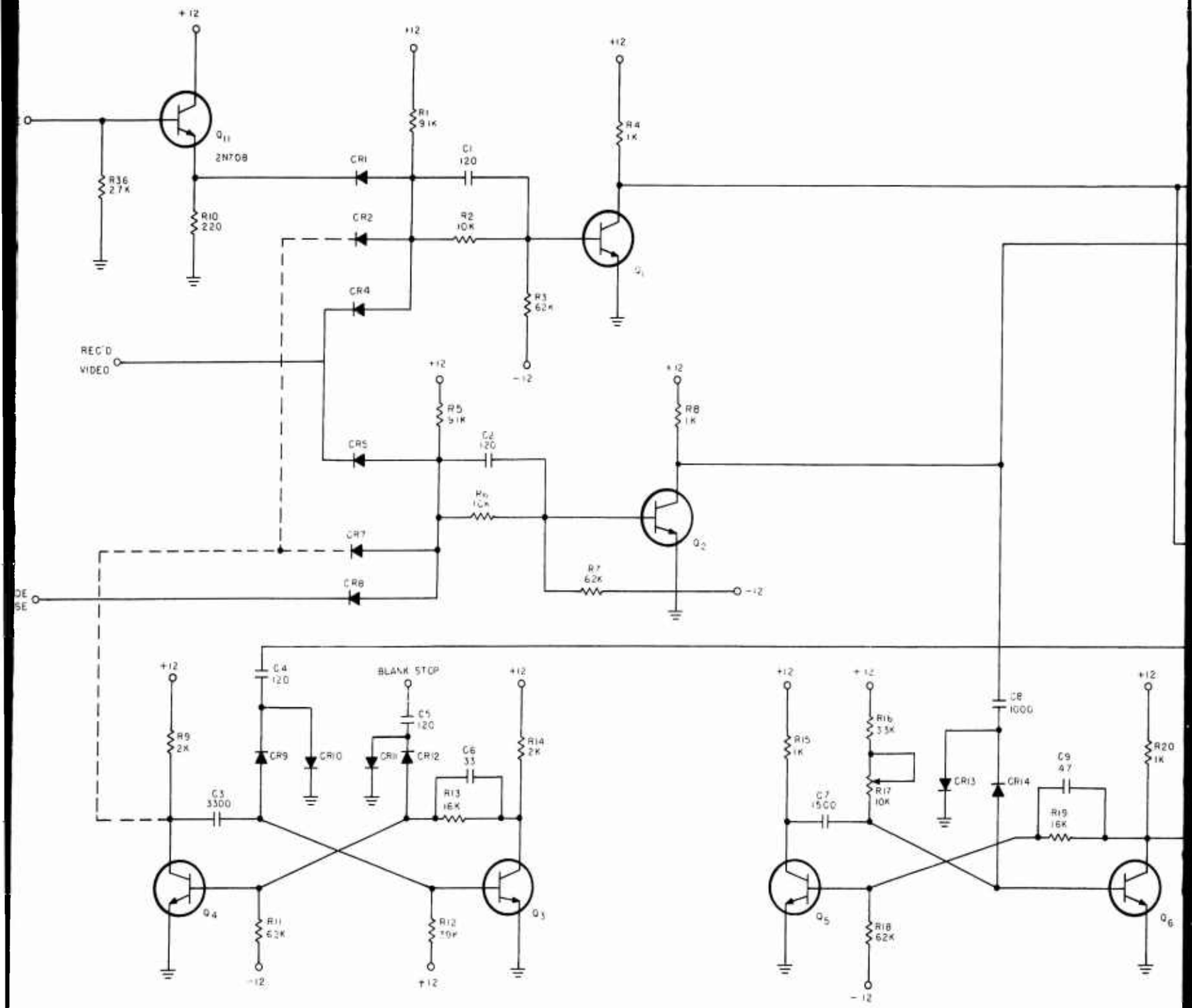
2. ALL CAPACITORS IN PF

3. ALL DIODES TYPE IN691.

4. ALL TRANSISTORS TYPE 2N708

5. DASHED INTERCONNECTION REMOVED FOR LAB TEST




+12
Q11
2N708
R36
27K
R10
220
CR1
CR2
CR4
R1
91K
C1
120
R2
10K
R3
62K
R4
1K
Q1
-12
REC'D
VIDEO
R5
91K
C2
120
CR5
CR7
CR8
R6
10K
R7
62K
R8
1K
Q2
BLANK STOP
C4
120
C5
120
R9
2K
CR9
CR10
CR11
CR12
C6
33
R13
16K
C3
3300
R14
2K
Q4
Q3
R11
6.2K
R12
39K
C8
1000
R15
1K
R16
33K
R17
10K
CR13
CR14
C9
47
R19
16K
C7
1500
R20
1K
Q5
Q6
R18
62K

2

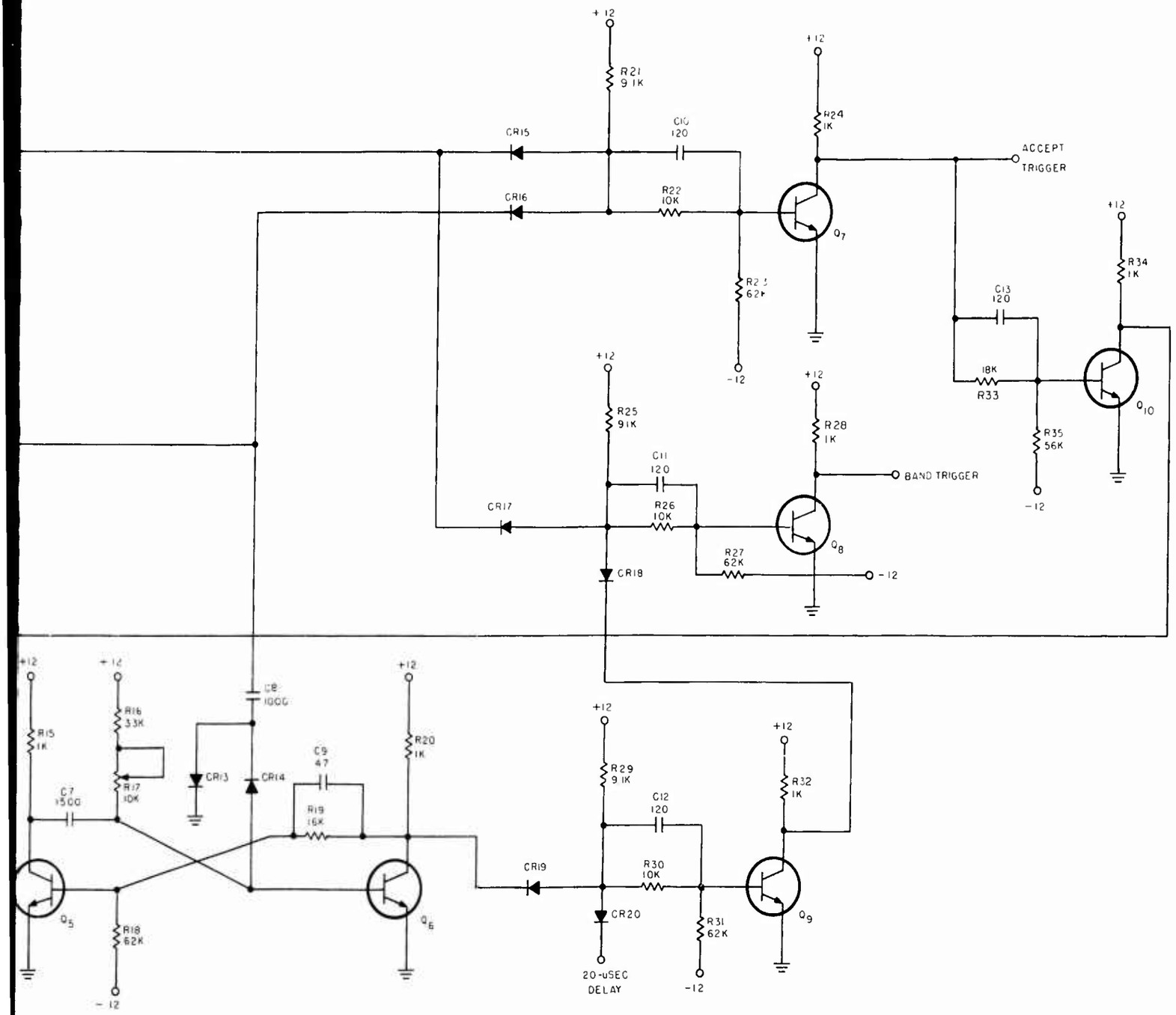
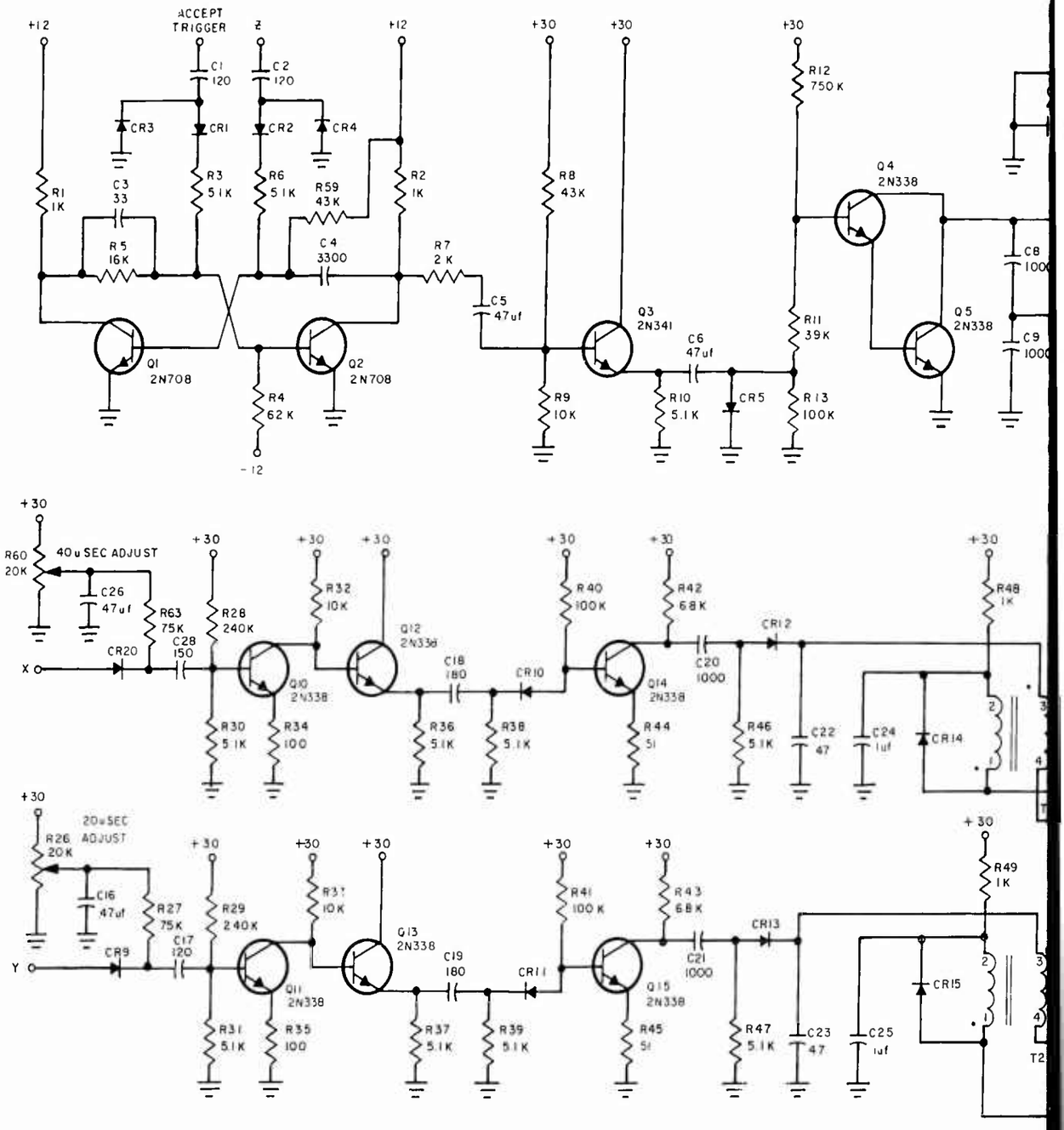
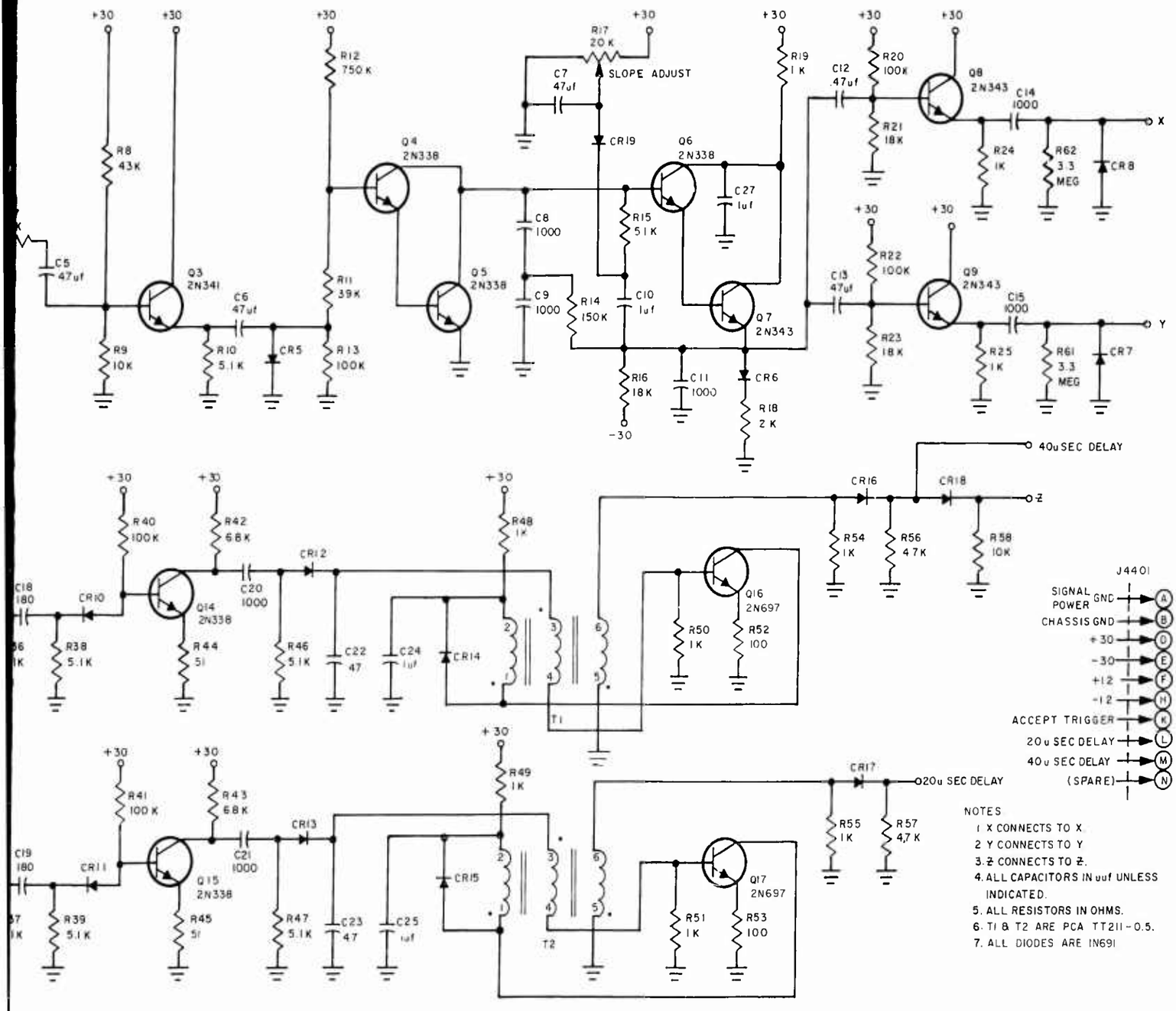


FIGURE 5-34
BAND DECODER (4300)


+12
ACCEPT TRIGGER
Z
+12
+30
+30
+30
C1 120
C2 120
CR3
CR1
CR2
CR4
R1 1K
C3 33
R3 5.1K
R6 5.1K
R59 43K
R2 1K
R8 43K
R12 750K
Q4 2N338
R5 16K
C4 3300
R7 2K
C5 47uf
Q3 2N341
C6 47uf
R11 39K
Q5 2N338
C8 1000
C9 1000
Q1 2N708
Q2 2N708
R4 62K
R9 10K
R10 5.1K
CR5
R13 100K
-12
+30
R60 20K
40u SEC ADJUST
C26 47uf
R63 75K
R28 240K
C28 150
CR20
X
R32 10K
Q12 2N338
C18 180
CR10
R40 100K
R42 6.8K
CR12
R48 1K
Q10 2N338
Q14 2N338
C20 1000
R30 5.1K
R34 100
R36 5.1K
R38 5.1K
R44 51
R46 5.1K
C22 47
C24 1uf
CR14
+30
R26 20K
20u SEC ADJUST
C16 47uf
R27 75K
R29 240K
C17 120
CR9
Y
R31 10K
Q13 2N338
C19 180
CR11
R41 100K
R43 6.8K
CR13
R49 1K
Q11 2N338
Q15 2N338
C21 1000
R31 5.1K
R35 100
R37 5.1K
R39 5.1K
R45 51
R47 5.1K
C23 47
C25 1uf
CR15
T2

1



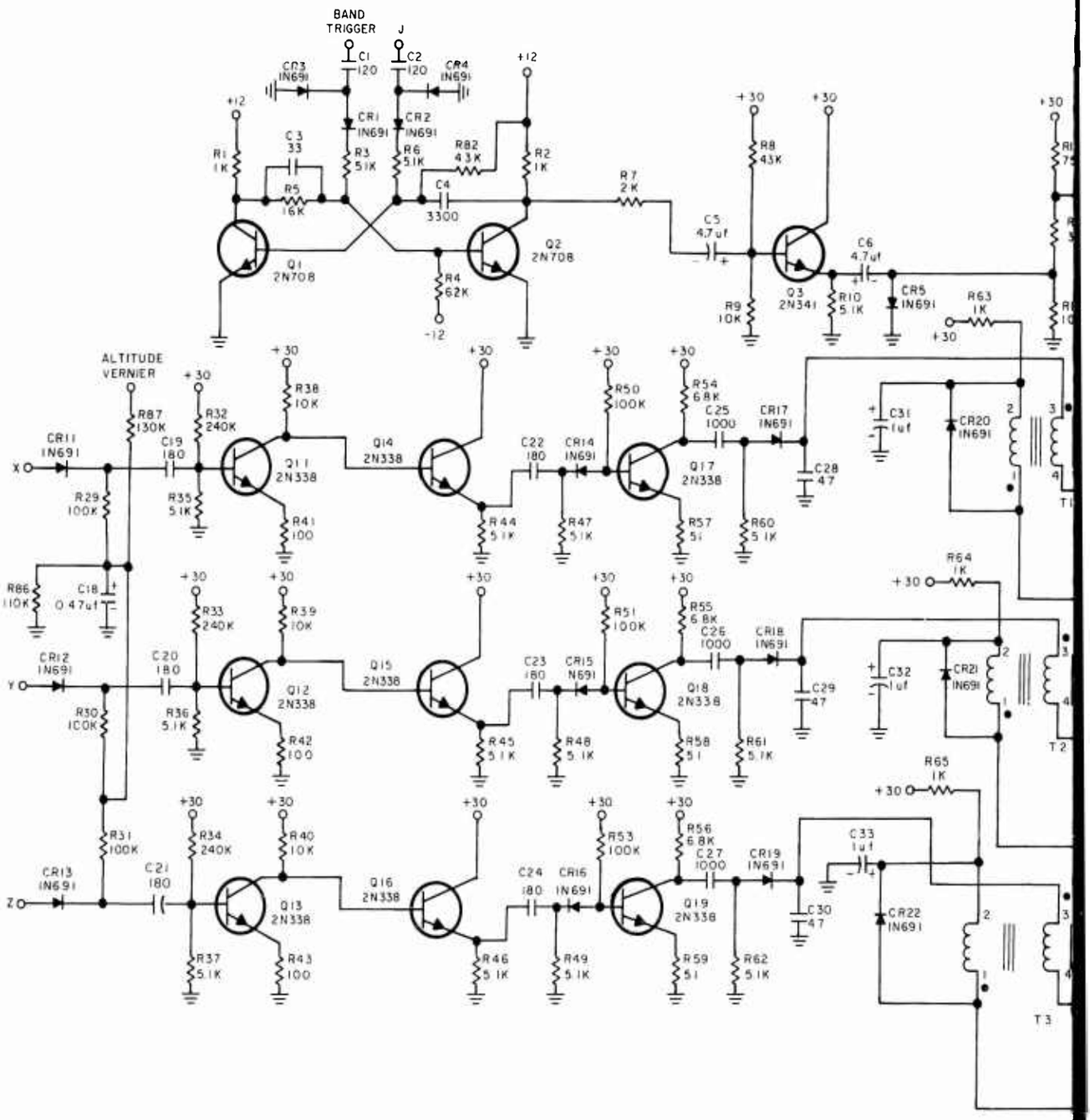
NOTES

1. X CONNECTS TO X.
2. Y CONNECTS TO Y
3. ~~Z~~ CONNECTS TO ~~Z~~.
4. ALL CAPACITORS IN uuf UNLESS INDICATED.
5. ALL RESISTORS IN OHMS.
6. T1 & T2 ARE PCA TT211-0.5.
7. ALL DIODES ARE IN691

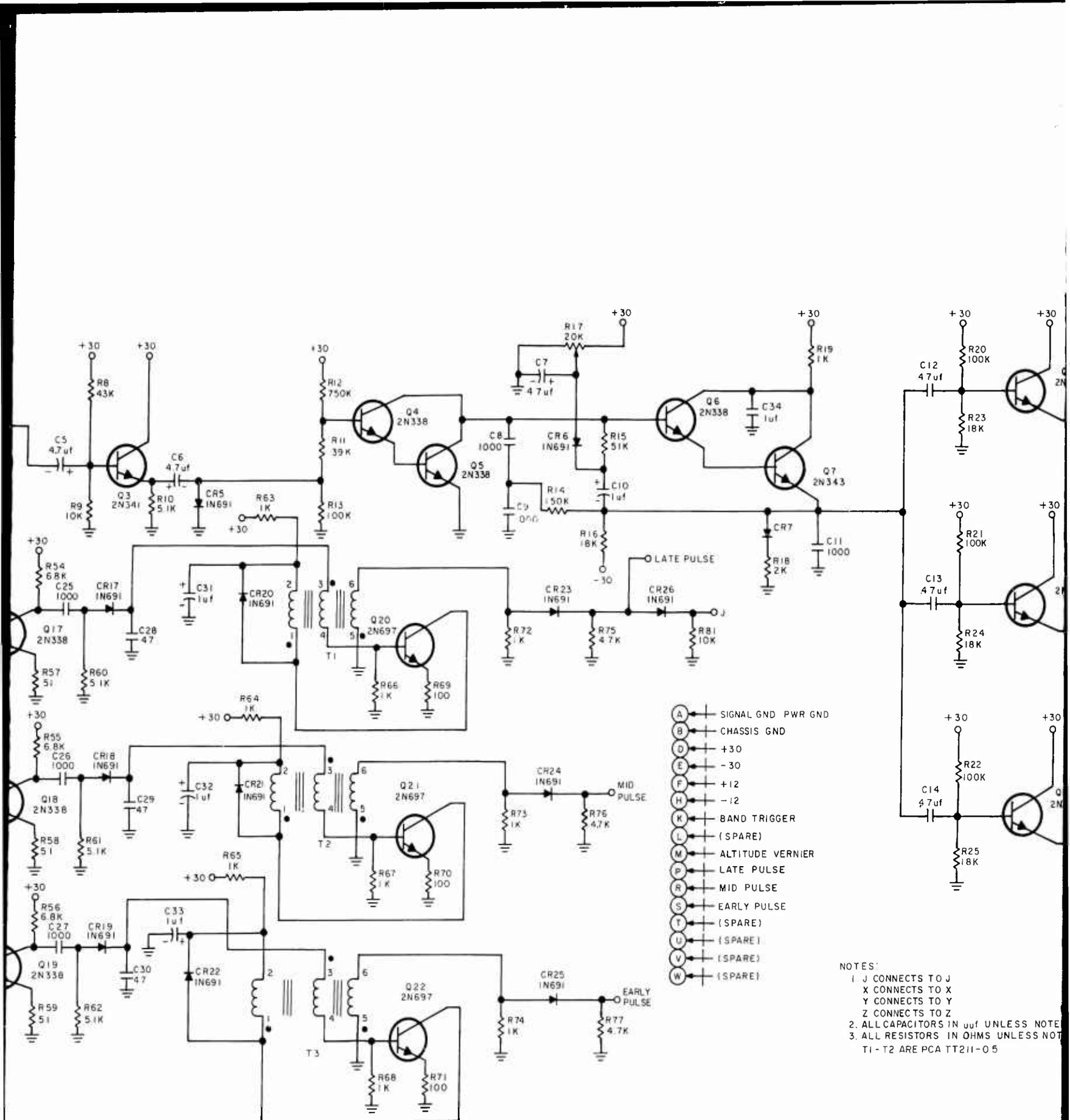
2

FIGURE 5-35

TWO-PULSE DELAY GENERATOR (4400)


BAND TRIGGER
J
C1 120
C2 120
CR3 IN691
CR4 IN691
CR1 IN691
CR2 IN691
+12
-12
R1 1K
C3 33
R5 16K
R3 51K
R6 5.1K
R82 43K
R2 1K
C4 3300
R4 62K
Q1 2N708
Q2 2N708
R7 2K
C5 4.7uf
R8 43K
R9 10K
Q3 2N341
C6 4.7uf
R10 5.1K
CR5 IN691
R63 1K
+30
ALTITUDE VERNIER
R87 130K
CR11 IN691
X
R29 100K
R86 110K
C18 0.47uf
C19 180
R32 240K
R35 5.1K
Q11 2N338
R38 10K
R41 100
Q14 2N338
C22 180
CR14 IN691
R44 5.1K
R47 5.1K
R50 100K
R54 6.8K
C25 1000
CR17 IN691
Q17 2N338
R57 51
R60 5.1K
C28 47
C31 1uf
CR20 IN691
T1
R64 1K
CR12 IN691
Y
R30 100K
C20 180
R33 240K
R36 5.1K
Q12 2N338
R39 10K
R42 100
Q15 2N338
C23 180
CR15 N691
R45 5.1K
R48 5.1K
R51 100K
R55 6.8K
C26 1000
CR18 IN691
Q18 2N338
R58 51
R61 5.1K
C29 47
C32 1uf
CR21 IN691
T2
R65 1K
CR13 IN691
Z
R31 100K
C21 180
R34 240K
R37 5.1K
Q13 2N338
R40 10K
R43 100
Q16 2N338
C24 180
CR16 IN691
R46 5.1K
R49 5.1K
R53 100K
R56 6.8K
C27 1000
CR19 IN691
Q19 2N338
R59 51
R62 5.1K
C30 47
C33 1uf
CR22 IN691
T3

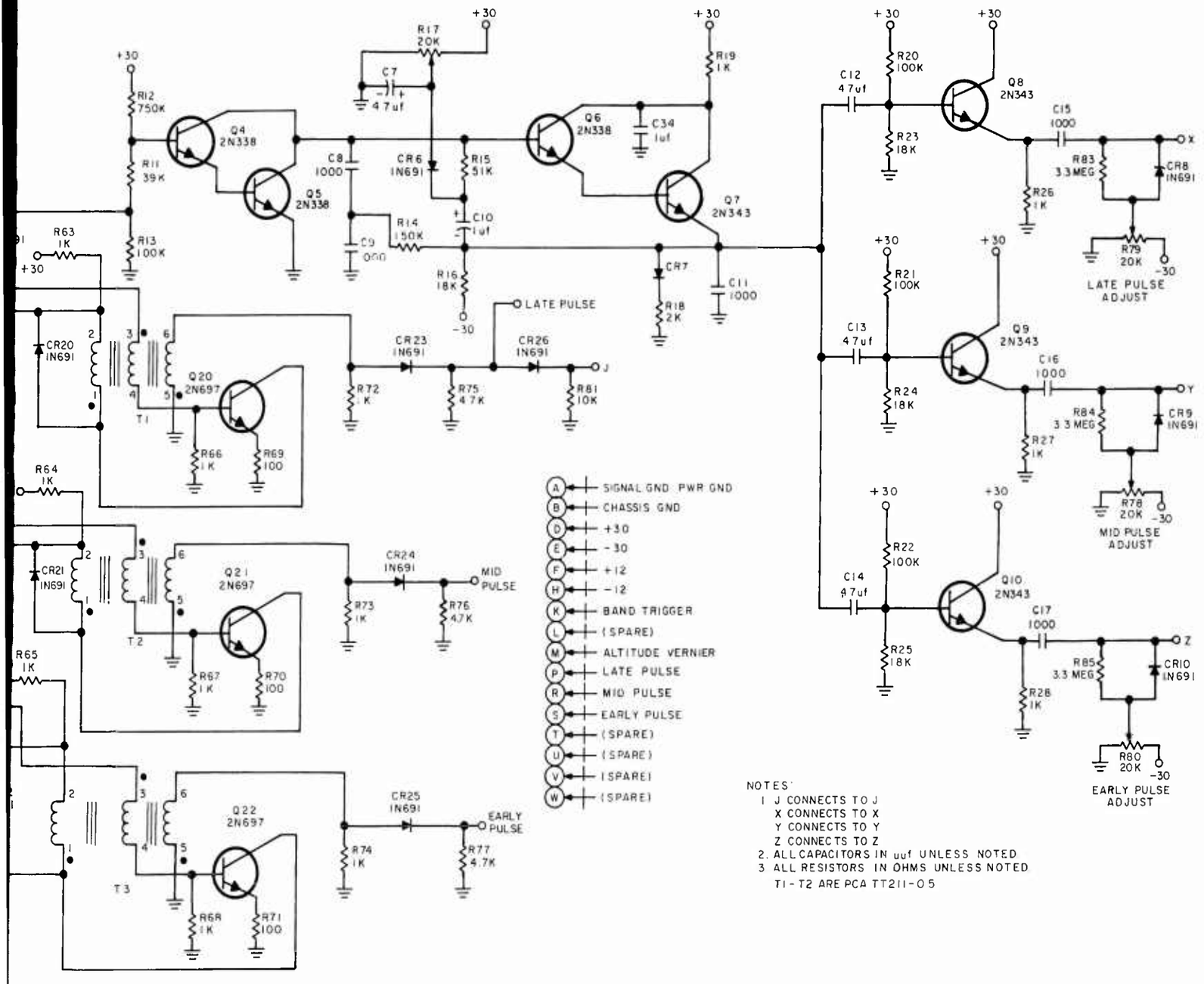

1



NOTES:
1. J CONNECTS TO J
   X CONNECTS TO X
   Y CONNECTS TO Y
   Z CONNECTS TO Z
2. ALL CAPACITORS IN uuf UNLESS NOTE
3. ALL RESISTORS IN OHMS UNLESS NOT
   T1 - T2 ARE PCA TT211-05

2

THREE-PULS

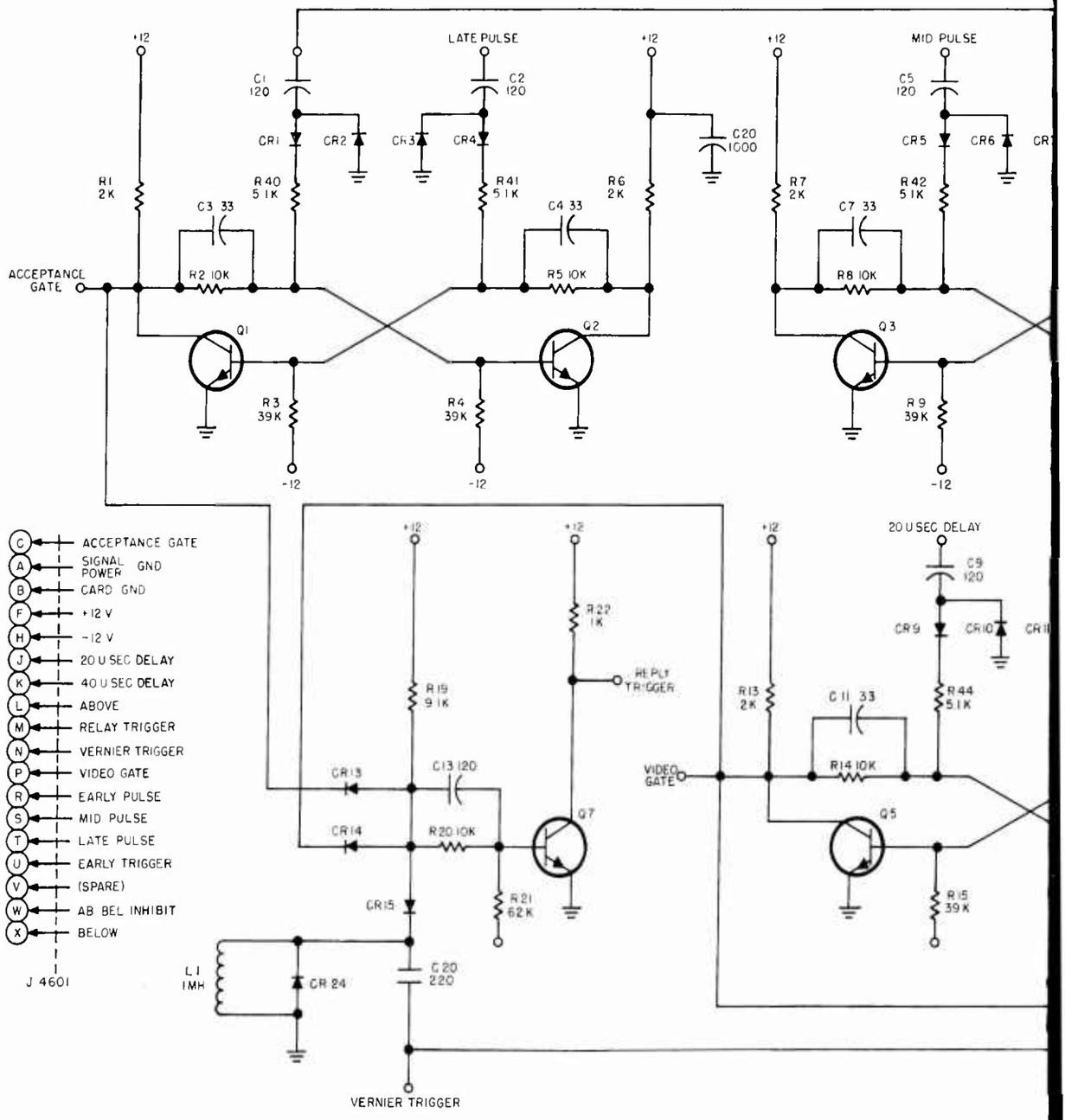


NOTES:
1. J CONNECTS TO J
   X CONNECTS TO X
   Y CONNECTS TO Y
   Z CONNECTS TO Z
2. ALL CAPACITORS IN uuf UNLESS NOTED
3. ALL RESISTORS IN OHMS UNLESS NOTED
   T1 - T2 ARE PCA TT211-05

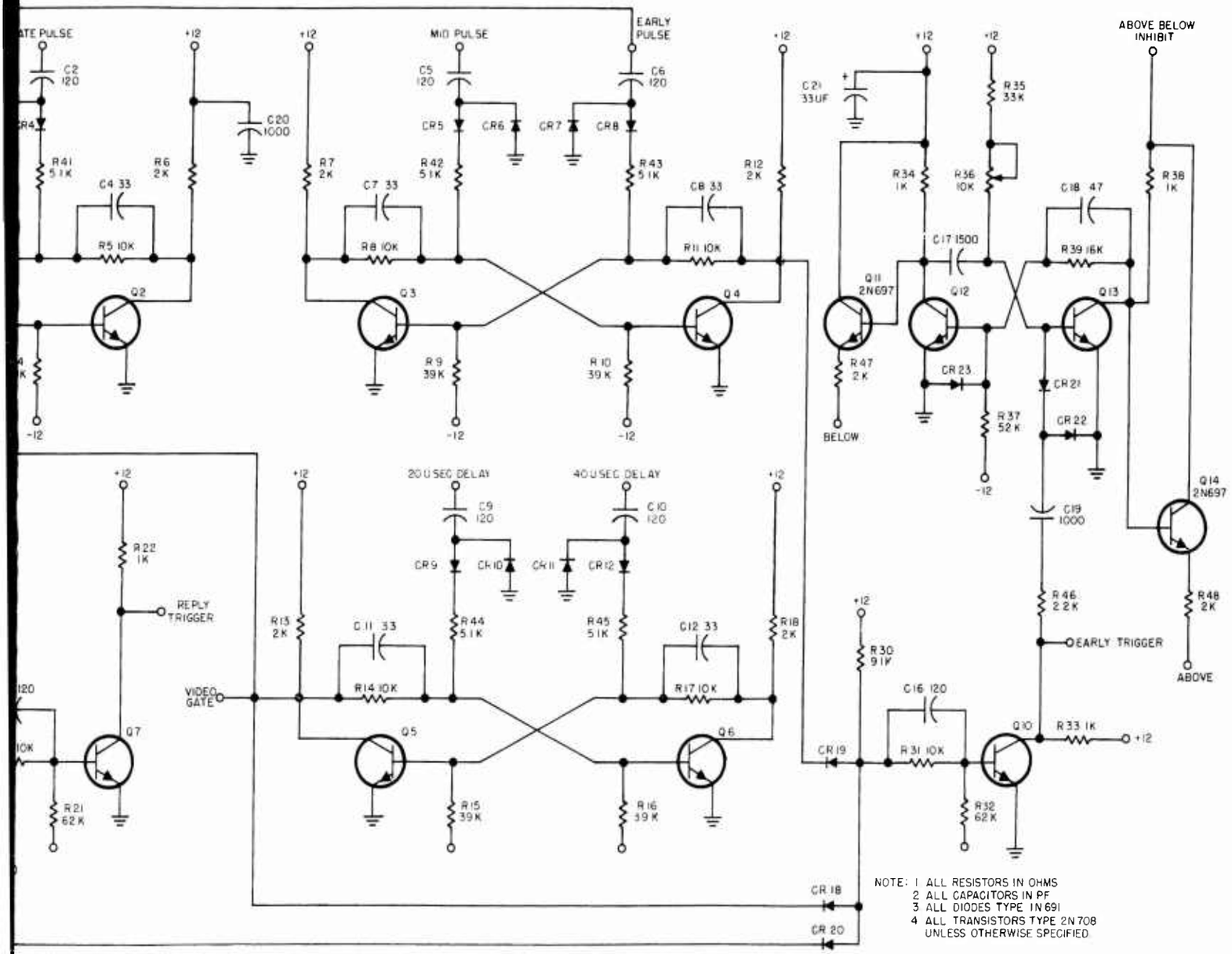
3

FIGURE 5-36

THREE-PULSE DELAY GENERATOR (4500)


+12
LATE PULSE
MID PULSE
C1 120
C2 120
C5 120
CR1
CR2
CR3
CR4
CR5
CR6
C20 1000
R1 2K
R40 5.1K
R41 5.1K
R6 2K
R7 2K
R42 5.1K
C3 33
C4 33
C7 33
ACCEPTANCE GATE
R2 10K
R5 10K
R8 10K
Q1
Q2
Q3
R3 39K
R4 39K
R9 39K
-12
C ACCEPTANCE GATE
A SIGNAL POWER GND
B CARD GND
F +12 V
H -12 V
J 20 U SEC DELAY
K 40 U SEC DELAY
L ABOVE
M RELAY TRIGGER
N VERNIER TRIGGER
P VIDEO GATE
R EARLY PULSE
S MID PULSE
T LATE PULSE
U EARLY TRIGGER
V (SPARE)
W AB BEL INHIBIT
X BELOW
J 4601
20 U SEC DELAY
C9 120
CR9
CR10
R22 1K
REPLY TRIGGER
R19 9.1K
R13 2K
C11 33
R44 5.1K
CR13
C13 120
VIDEO GATE
R14 10K
CR14
R20 10K
Q7
Q5
CR15
R21 62K
R15 39K
L1 1MH
CR 24
C20 220
VERNIER TRIGGER

1



NOTE: 1 ALL RESISTORS IN OHMS
2 ALL CAPACITORS IN PF
3 ALL DIODES TYPE IN691
4 ALL TRANSISTORS TYPE 2N708 UNLESS OTHERWISE SPECIFIED

2

FIGURE 5-37

VERNIER-DECODER (4600)

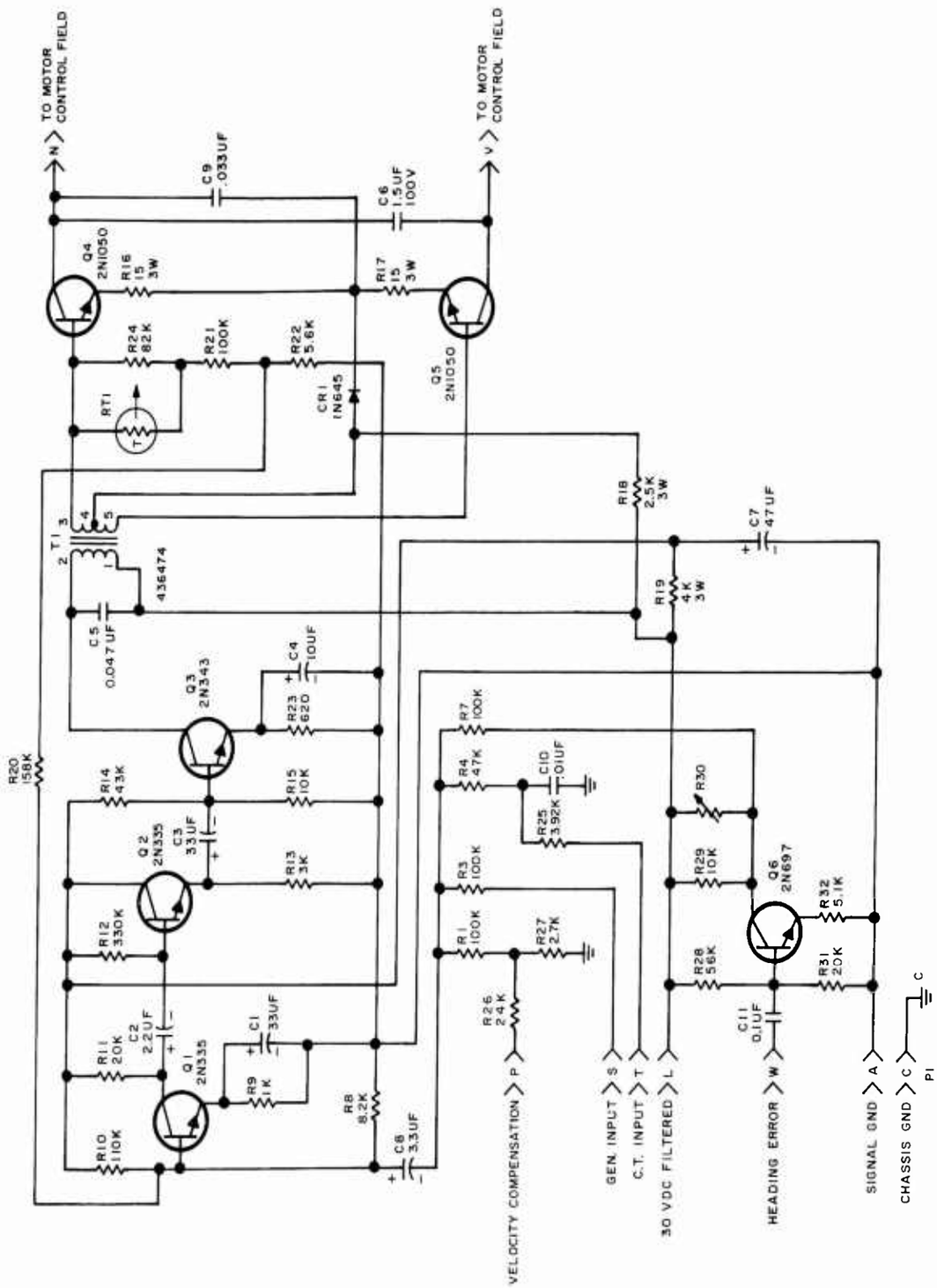


FIGURE 5-38. A-1 MAGNETIC BEARING MOTOR AMPLIFIER

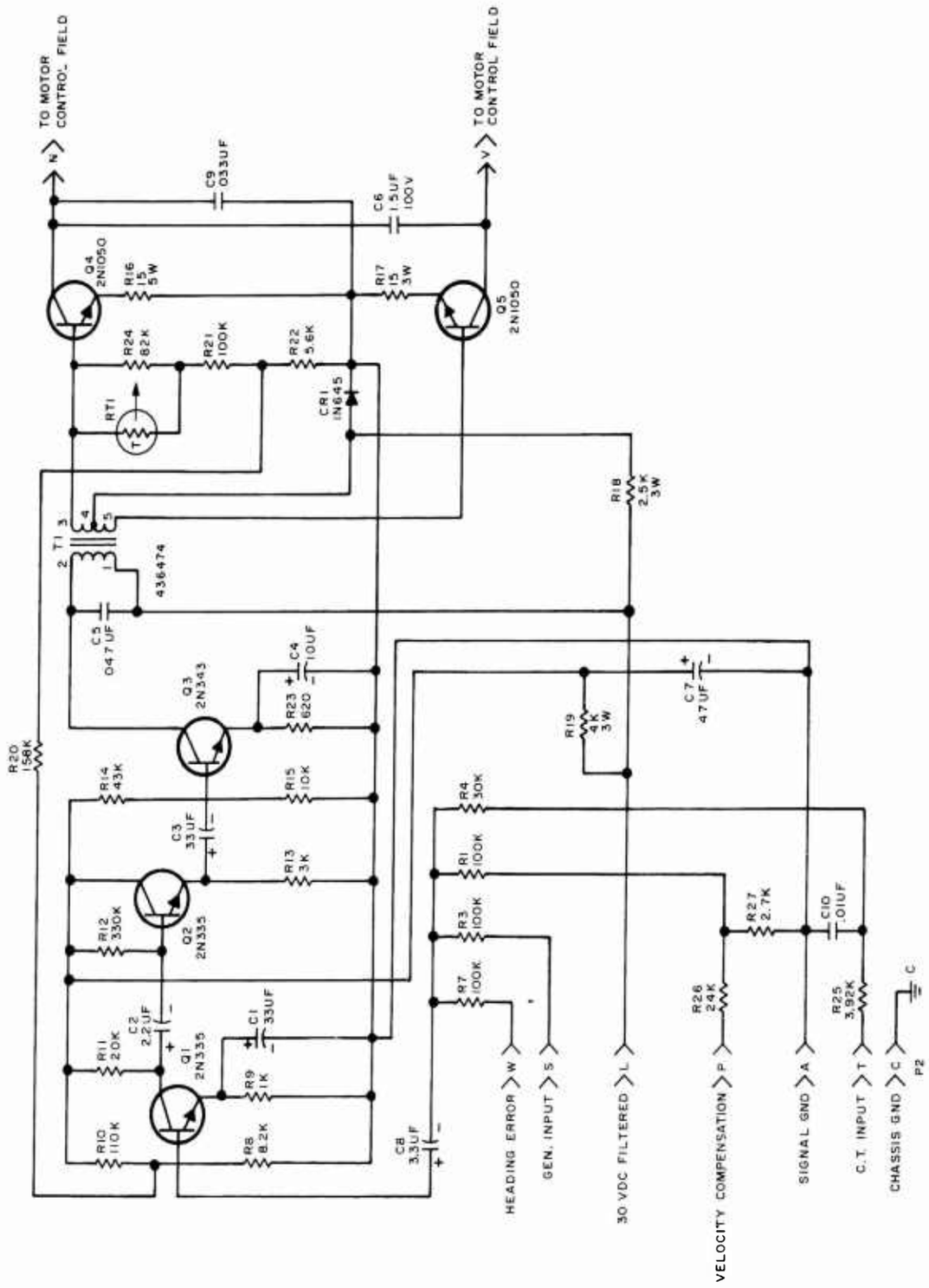
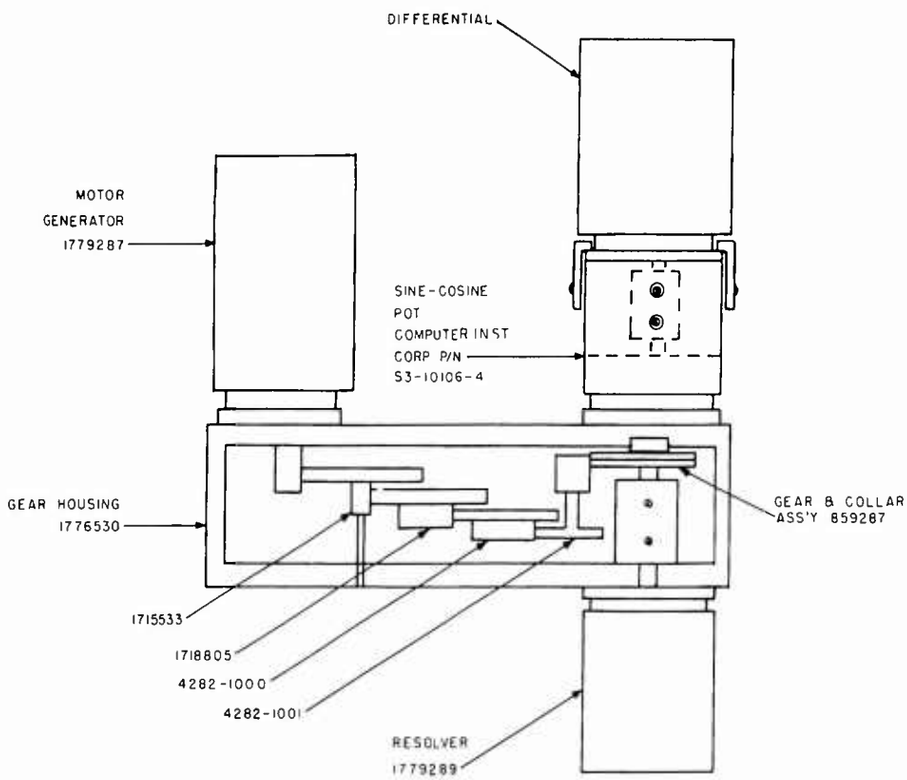
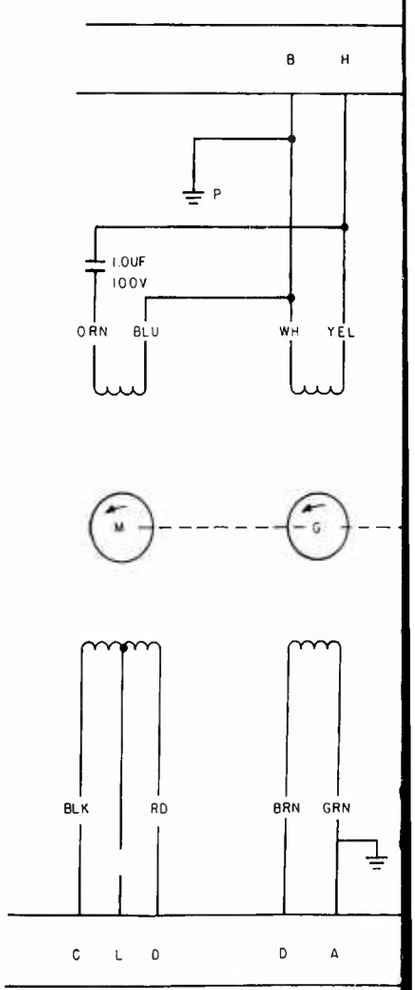


FIGURE 5-39. A-2 RELATIVE BEARING MOTOR AMPLIFIER

KEARFOTT
RS9114A
TRANSMITTE





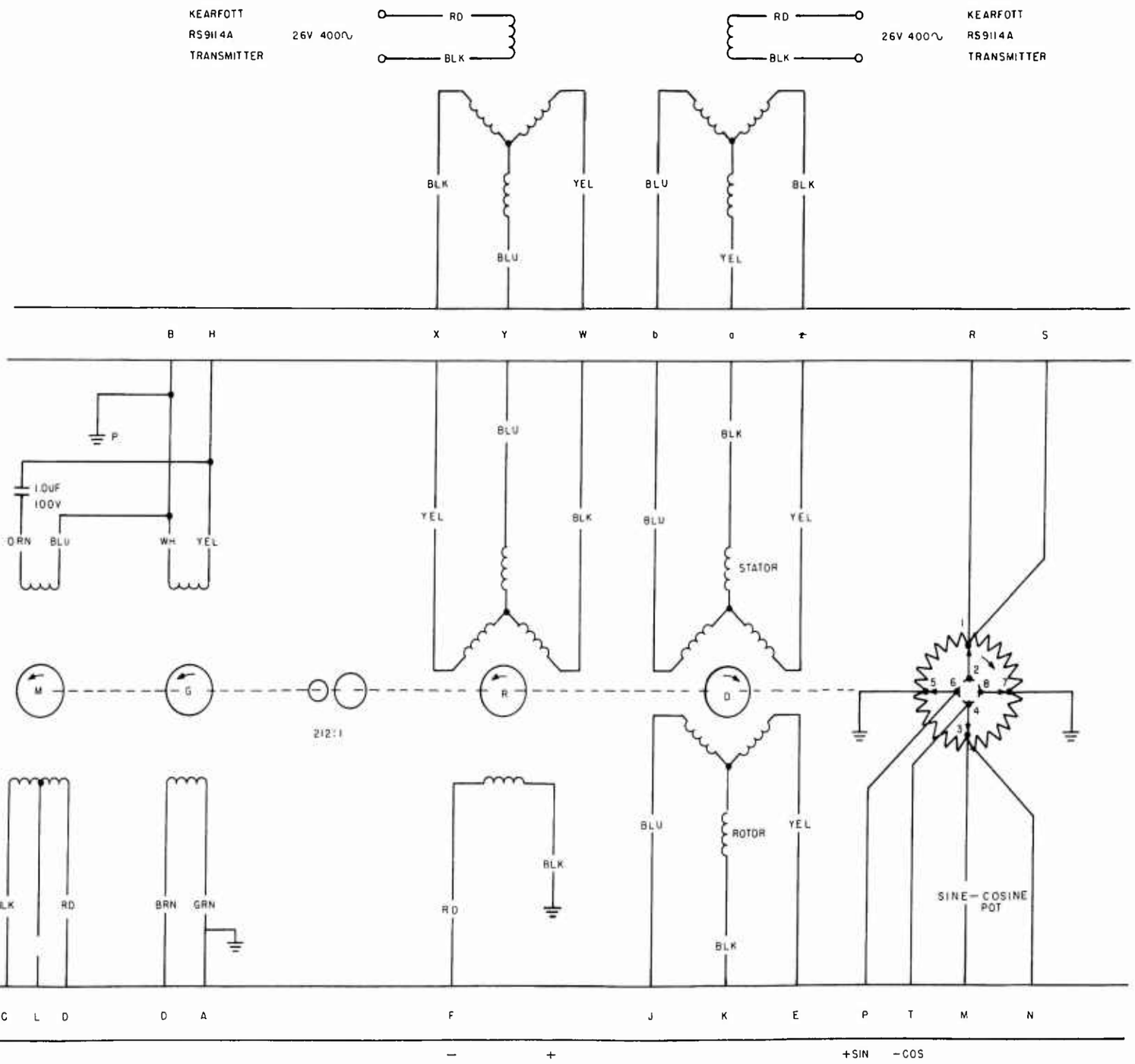
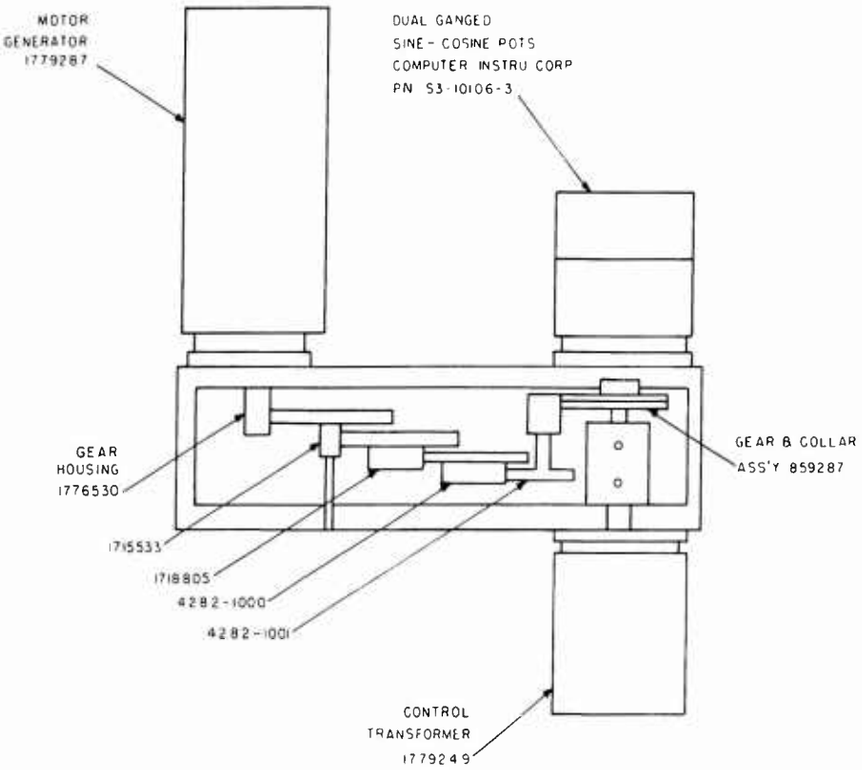
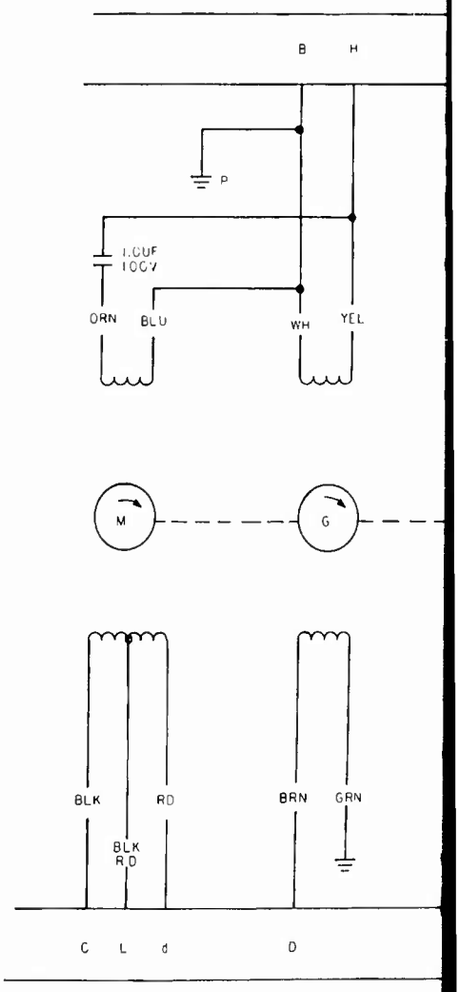


FIGURE 5-40
A-3 RELATIVE BEARING SERVO


MOTOR
GENERATOR
1779287
DUAL GANGED
SINE - COSINE POTS
COMPUTER INSTRU CORP
PN 53-10106-3
GEAR
HOUSING
1776530
GEAR & COLLAR
ASS'Y 859287
1715533
1718805
4282-1000
4282-1001
CONTROL
TRANSFORMER
1779249


B
H
P
1.0UF
100V
ORN
BLU
WH
YEL
M
G
BLK
RD
BLK
RD
BRN
GRN
C
L
d
D

1

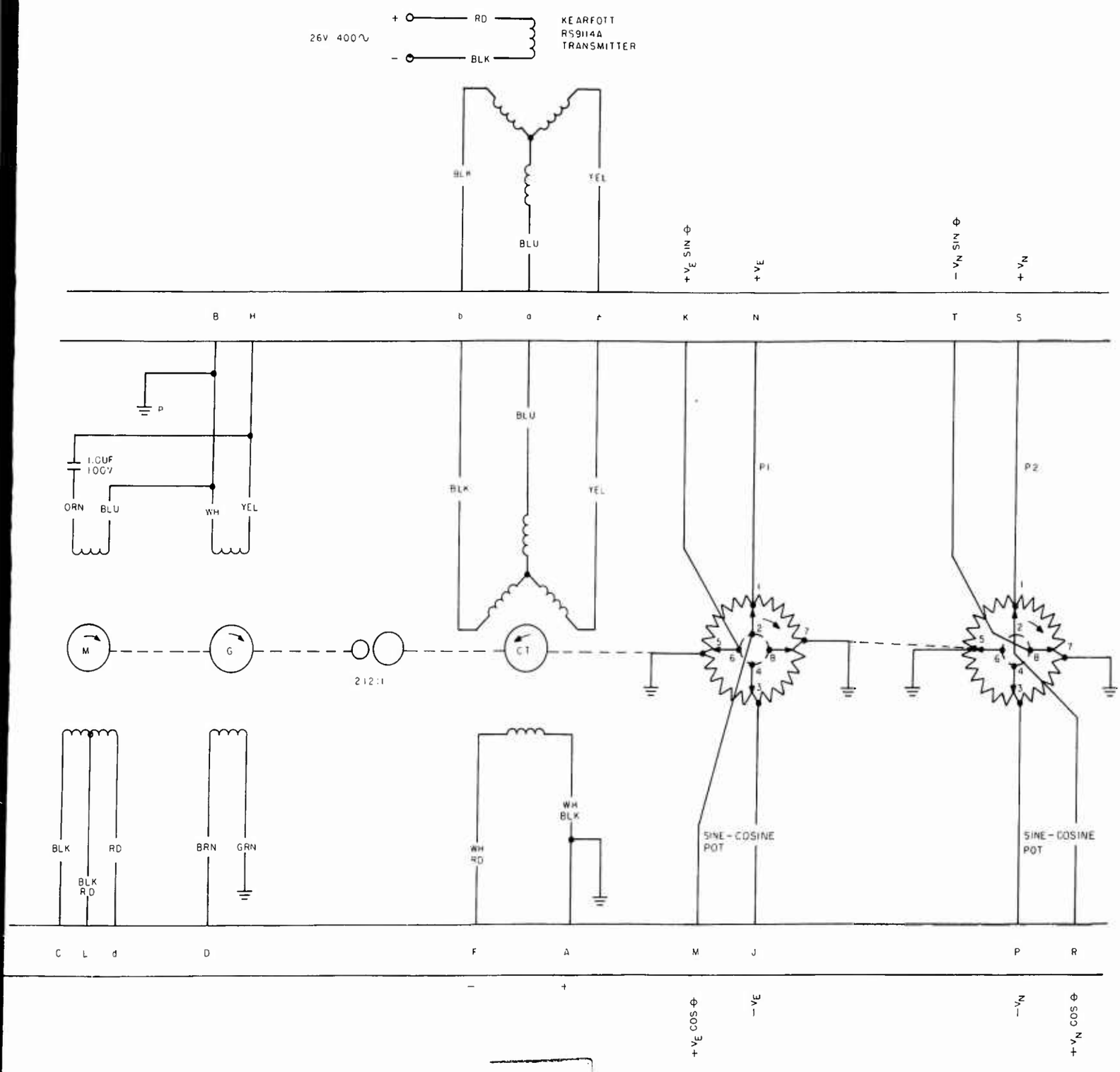
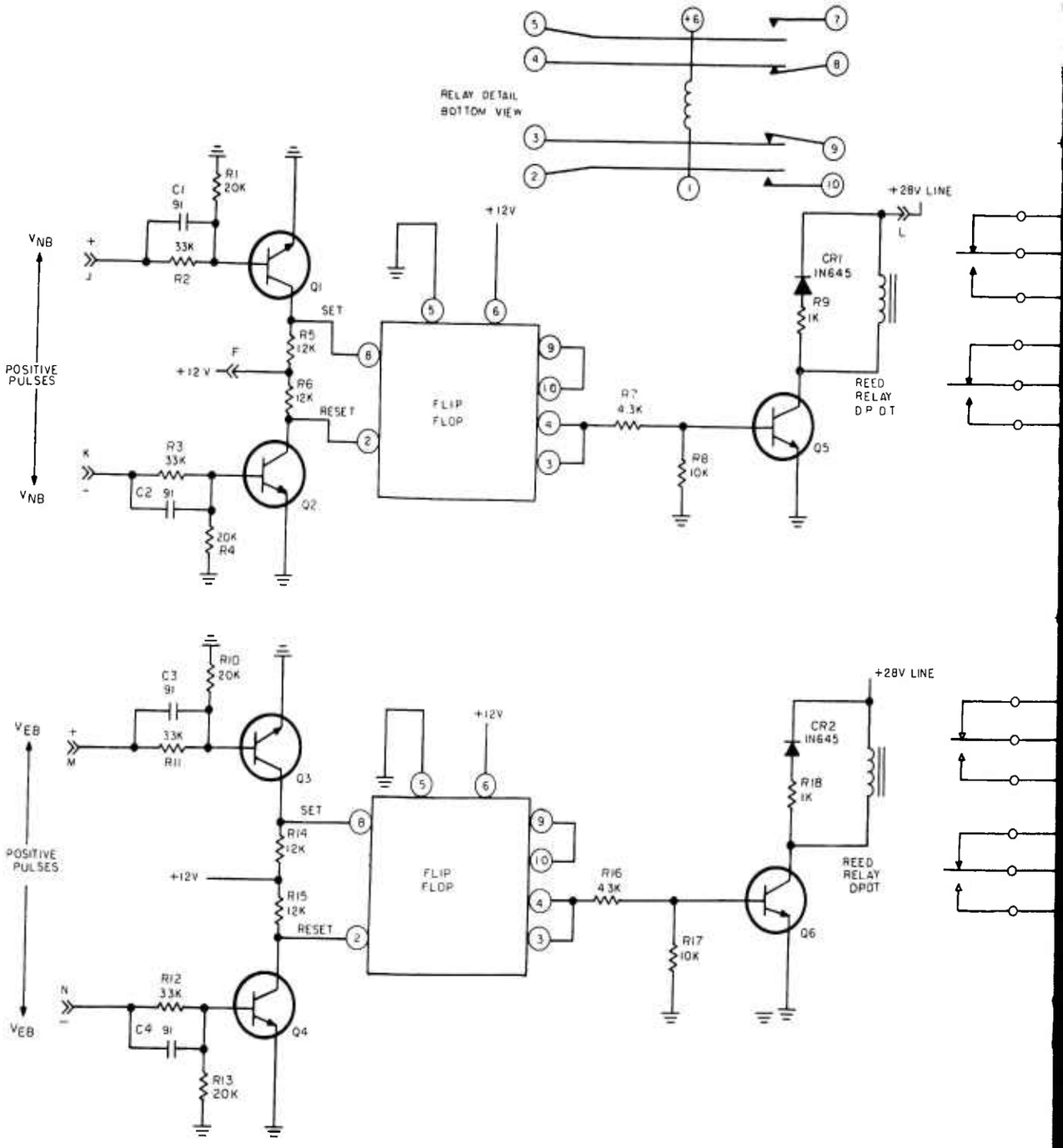


FIGURE 5-41

A-4 MAGNETIC BEARING SERVO

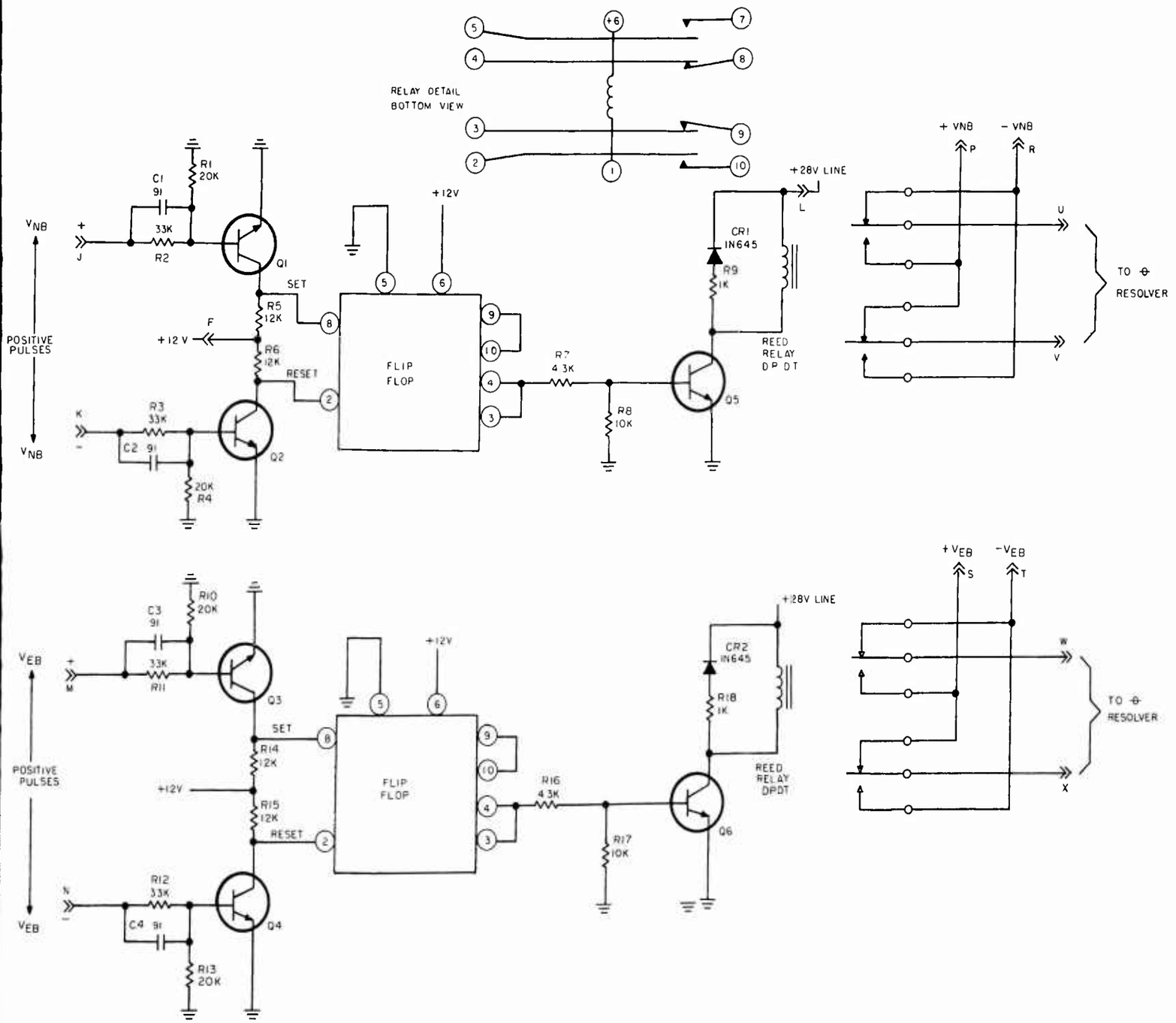


Q_1, Q_2, Q_3, Q_4, ---------- 2N697

Q_5, Q_6 ---------- 2N2087

NOTE: RELAY SHOWN IN DE-ENERGIZED STATE.
CAPACITORS ARE IN pf

1



Q_1, Q_2, Q_3, Q_4, _____ 2N697

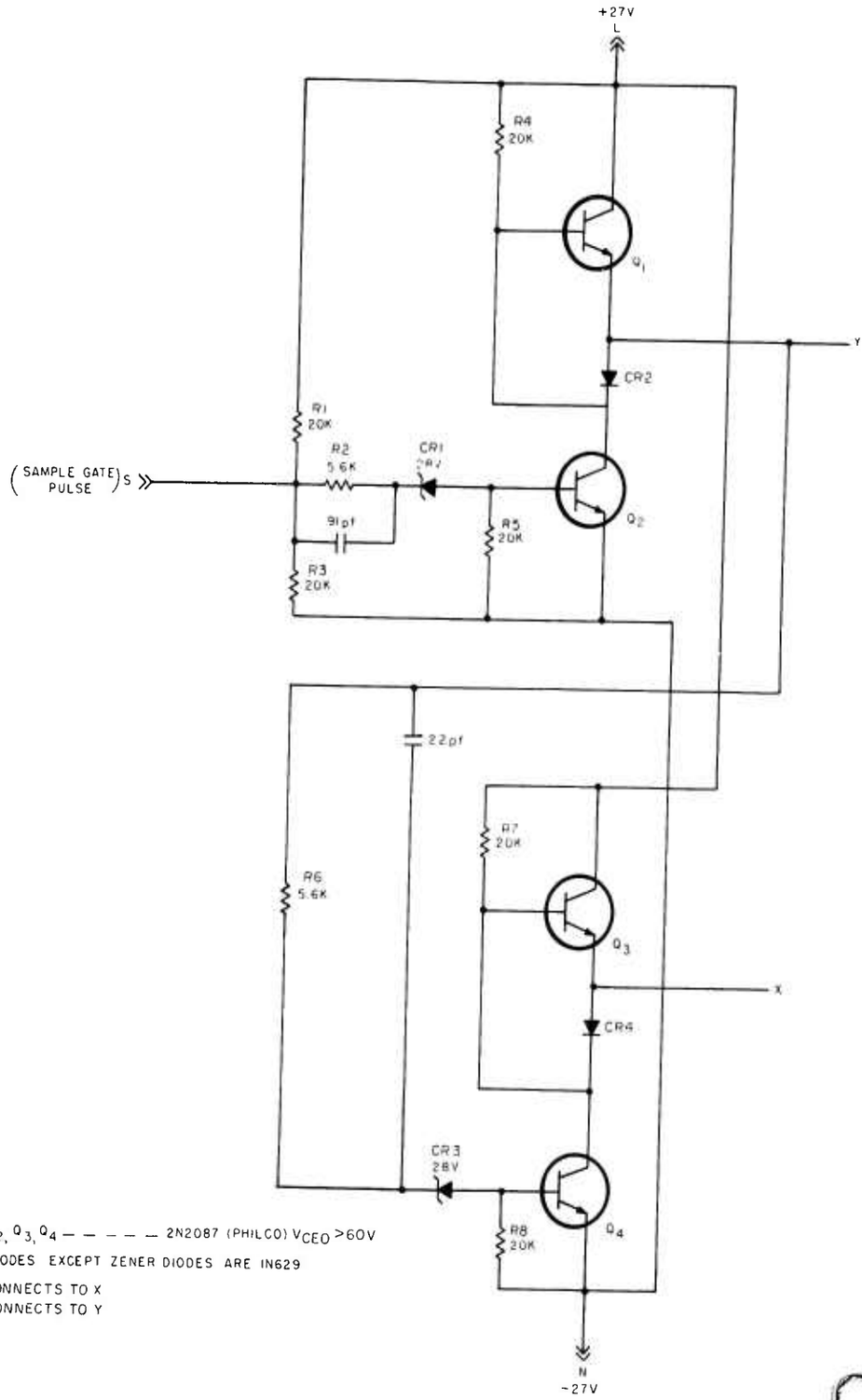
Q_5, Q_6 _____ 2N2087

NOTE: RELAY SHOWN IN DE-ENERGIZED STATE
CAPACITORS ARE IN pf

2

FIGURE 5-42

A-5 POLARITY CONTROL CIRCUIT



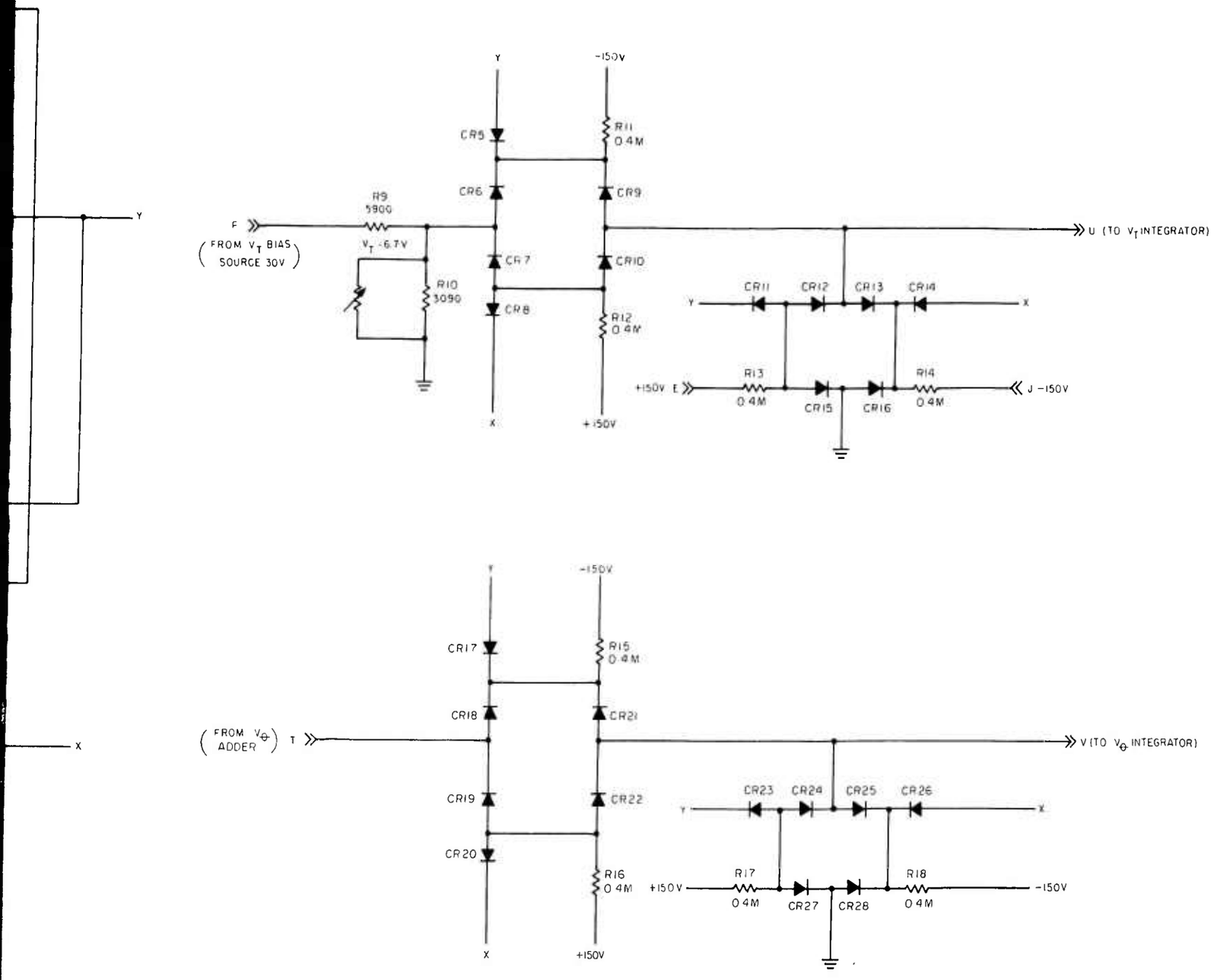
Q_1, Q_2, Q_3, Q_4 — — — — — 2N2087 (PHILCO) $V_{CEO} > 60V$

ALL DIODES EXCEPT ZENER DIODES ARE IN629

X CONNECTS TO X

Y CONNECTS TO Y

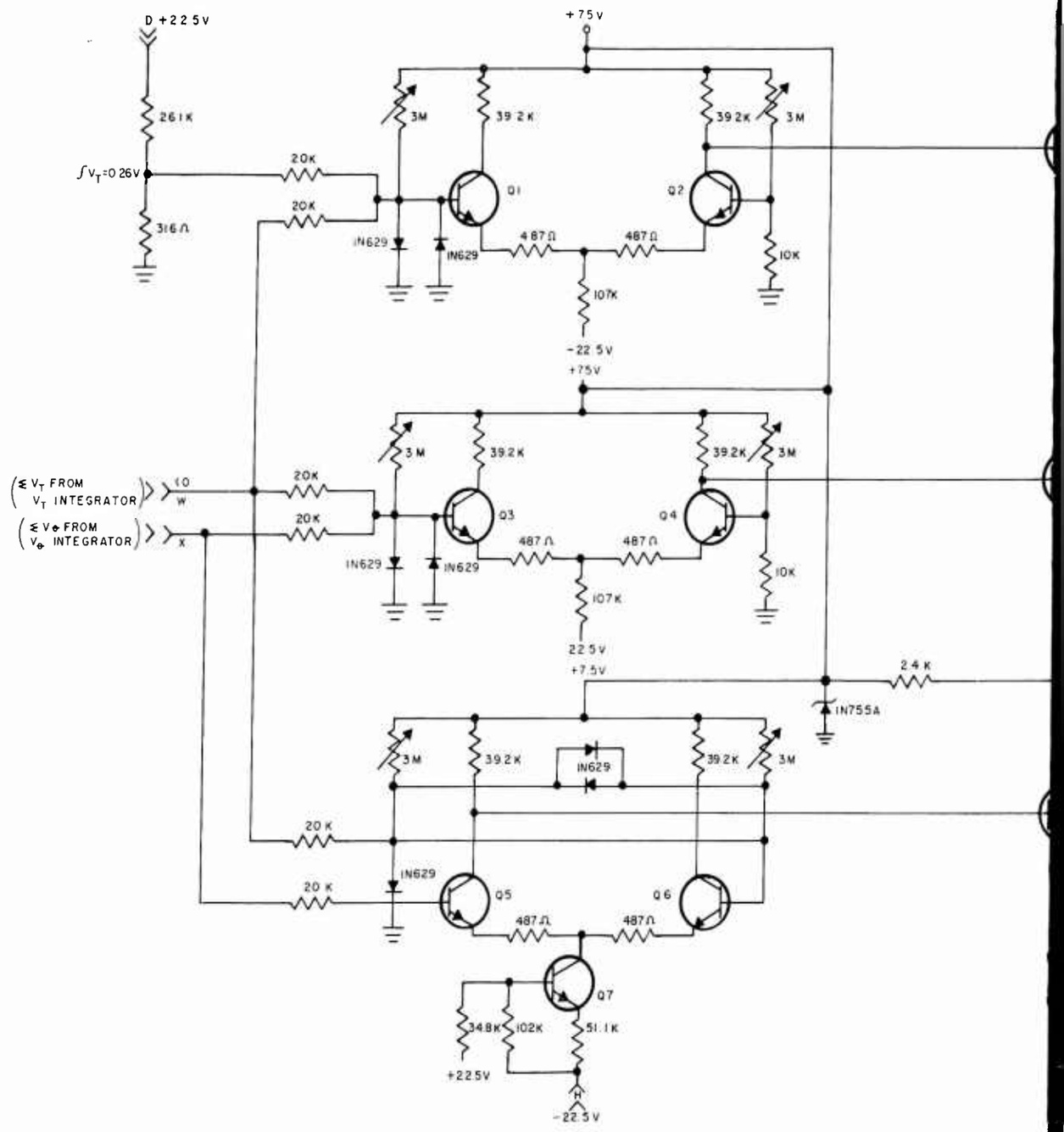
1



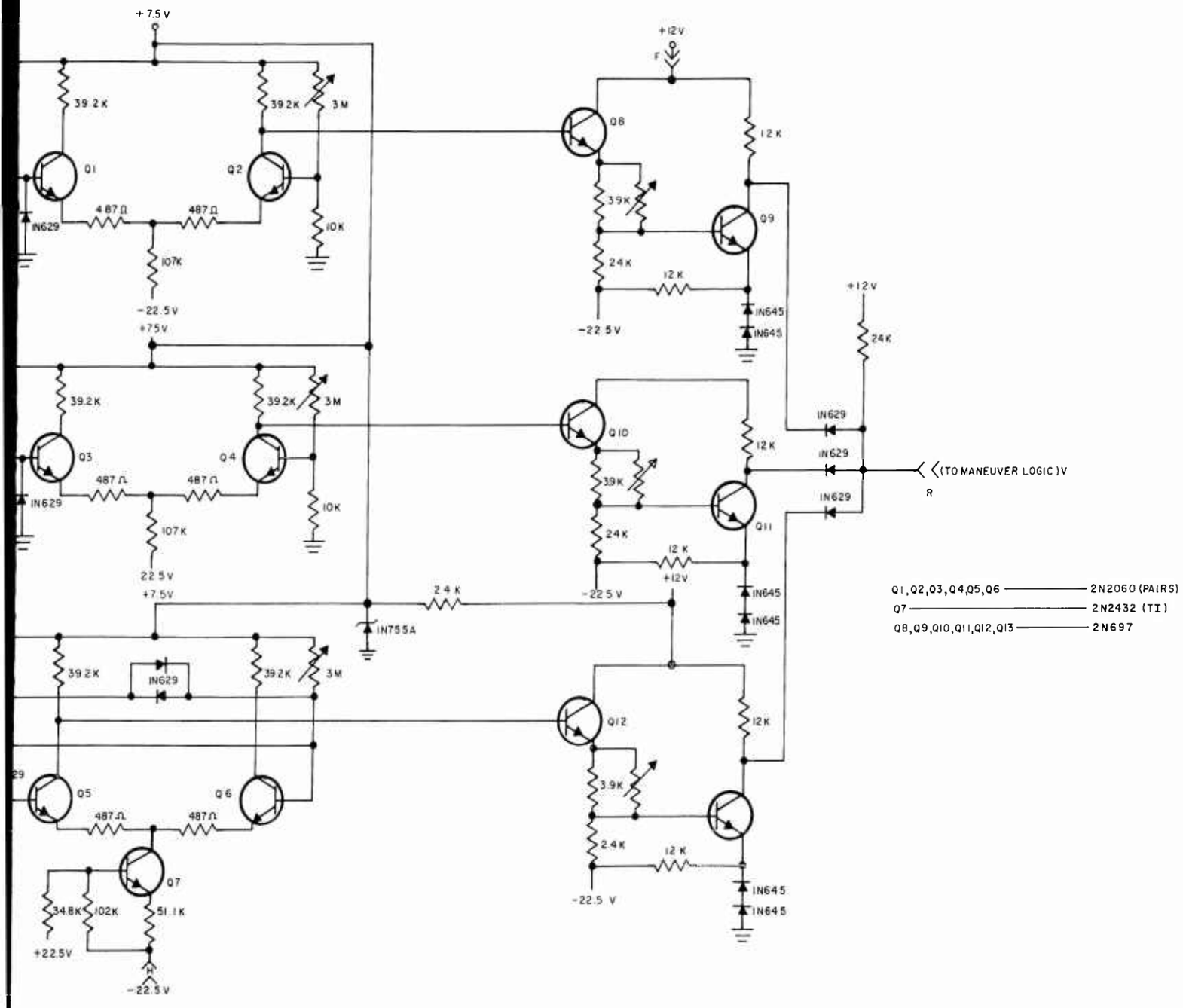
2

FIGURE 5-43

A-6 NORMAL VELOCITY CRITERION COMPARATOR AND SAMPLE GATE CONTROLLER (SHEET 1 OF 2)


D +22.5V
261K
∫V_T=0.26V
316Ω
20K
20K
3M
39.2K
Q1
IN629
IN629
487Ω
487Ω
39.2K
3M
Q2
10K
107K
-22.5V
+7.5V
(≤ V_T FROM V_T INTEGRATOR)
(≤ V_φ FROM V_φ INTEGRATOR)
W
X
Q3
Q4
2.4K
IN755A
Q5
Q6
Q7
34.8K
102K
51.1K
+22.5V
R
-22.5V

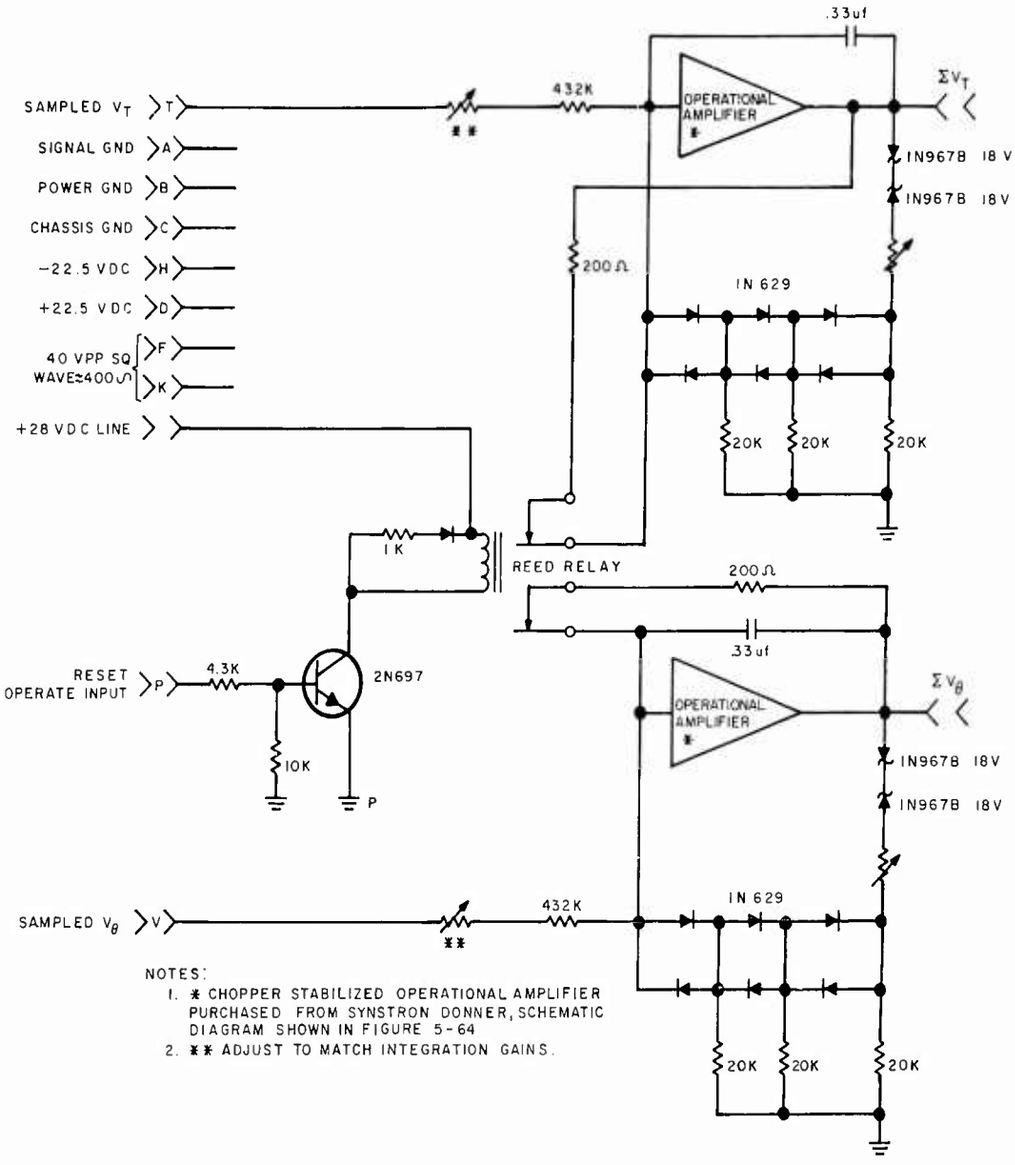

1



2

FIGURE 5-43

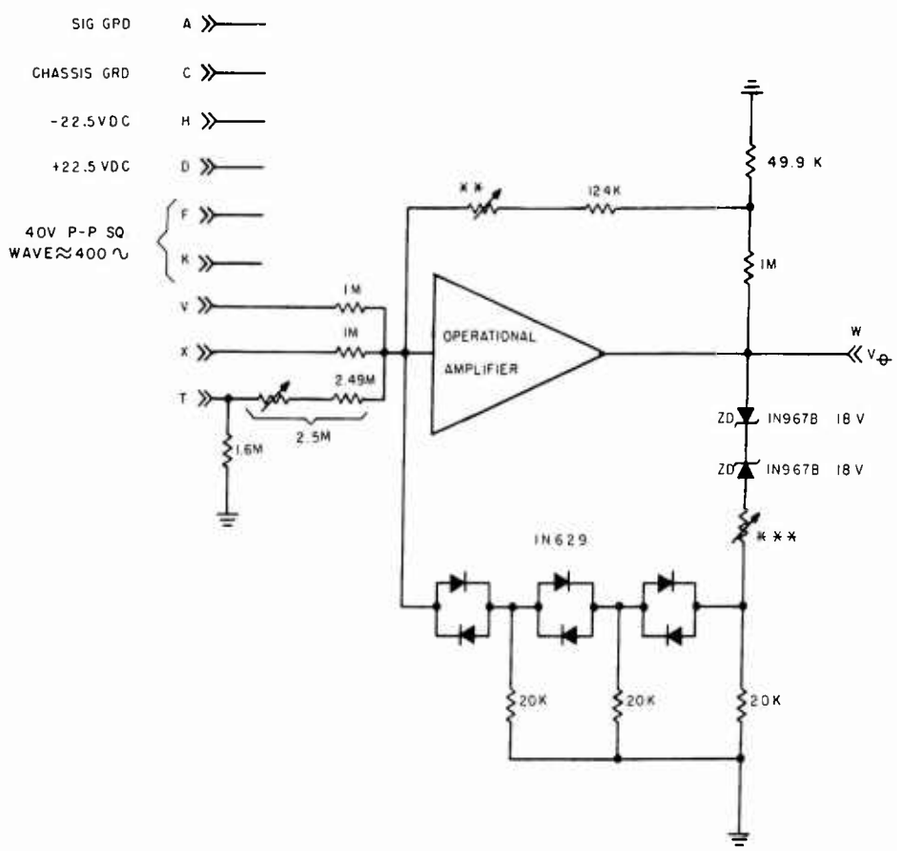
A-6 NORMAL VELOCITY CRITERION COMPARATOR AND SAMPLE GATE CONTROLLER (SHEET 2 OF 2)



NOTES:

1. * CHOPPER STABILIZED OPERATIONAL AMPLIFIER PURCHASED FROM SYNSTRON DONNER, SCHEMATIC DIAGRAM SHOWN IN FIGURE 5-64
2. ** ADJUST TO MATCH INTEGRATION GAINS.

FIGURE 5-44. A-7 VELOCITY INTEGRATORS

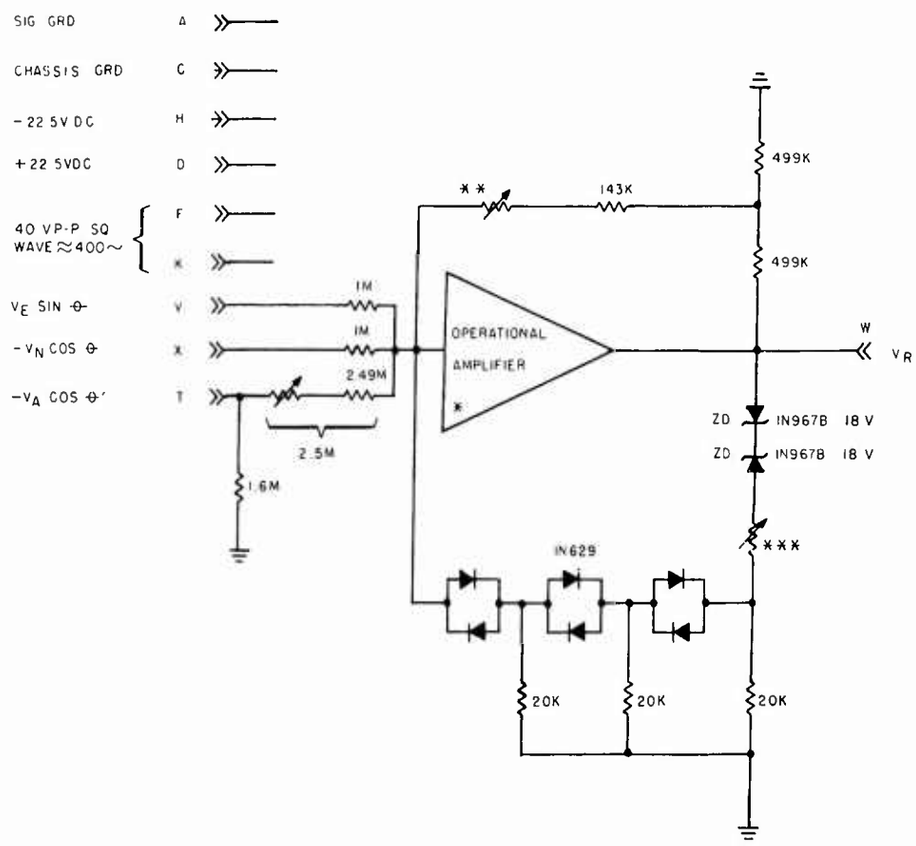


* CHOPPER STABILIZED OPERATIONAL AMPLIFIER. PURCHASED FROM SYNSTRON DONNER. SCHEMATIC DIAGRAM OF AMPLIFIER SHOWN IN FIGURE 5-64

* * ADJUSTED TO PRODUCE VOLTAGE GAIN OF 3.76 V/V FROM 1-MEG INPUTS.

* * * ADJUSTS LIMIT VOLTAGE ≈ 0.15 V/KΩ

FIGURE 5-45. A-8 NORMAL VELOCITY ADDER

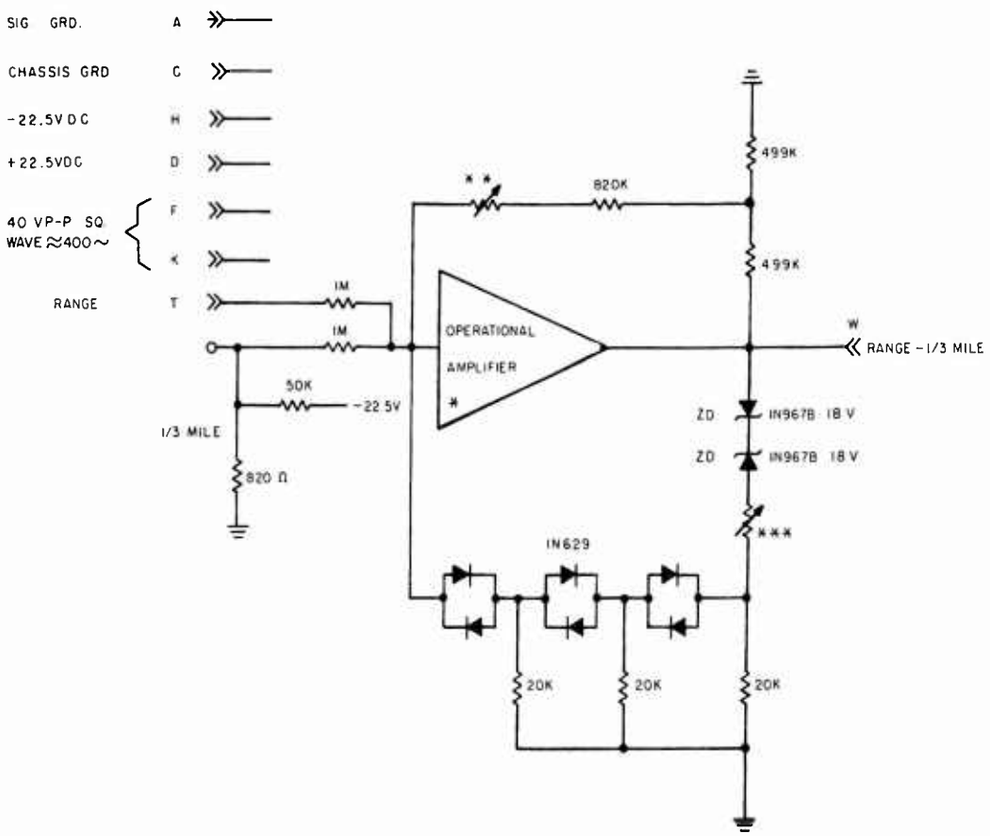


* CHOPPER STABILIZED OPERATIONAL AMPLIFIER. PURCHASED FROM SYNSTRON DONNER. SCHEMATIC DIAGRAM OF AMPLIFIER SHOWN IN FIGURE 5-64

** ADJUSTED TO PRODUCE VOLTAGE GAIN OF 0.794 V/V FROM 1-MEG. INPUTS.

*** ADJUSTS LIMIT VOLTAGE ≈ 0.15V/KΩ

FIGURE 5-46. A-9 RADIAL VELOCITY ADDER



* CHOPPER STABILIZED OPERATIONAL AMPLIFIER. PURCHASED FROM SYNSTRON DONNER. SCHEMATIC DIAGRAM OF AMPLIFIER SHOWN IN FIGURE 5-64.

** ADJUST TO PRODUCE VOLTAGE GAIN OF 2.14 V/V FROM 1-MEG. INPUTS.

*** ADJUST LIMIT VOLTAGE $\approx$ 0.15 V/KΩ

FIGURE 5-47. A-10 RANGE ADDER

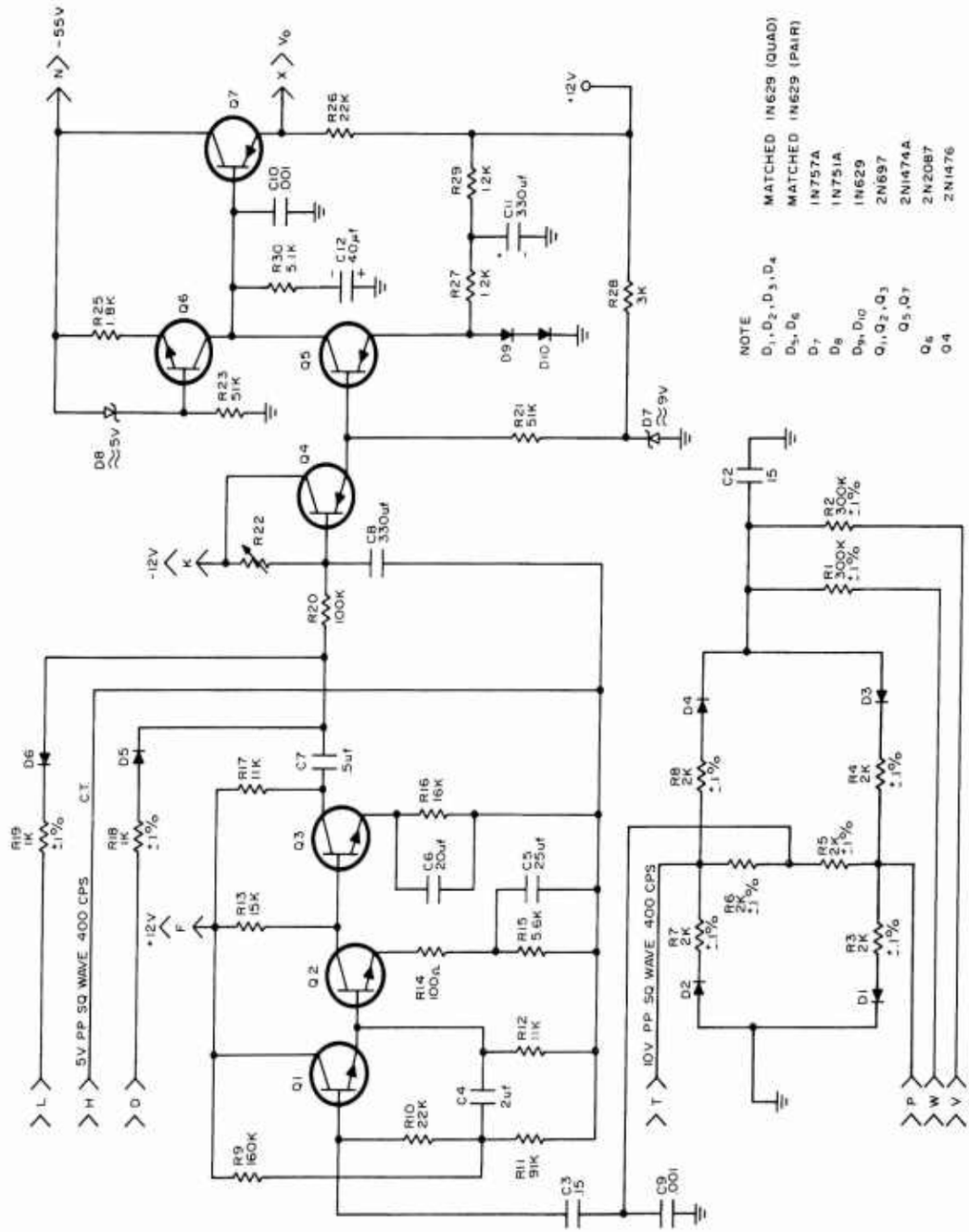
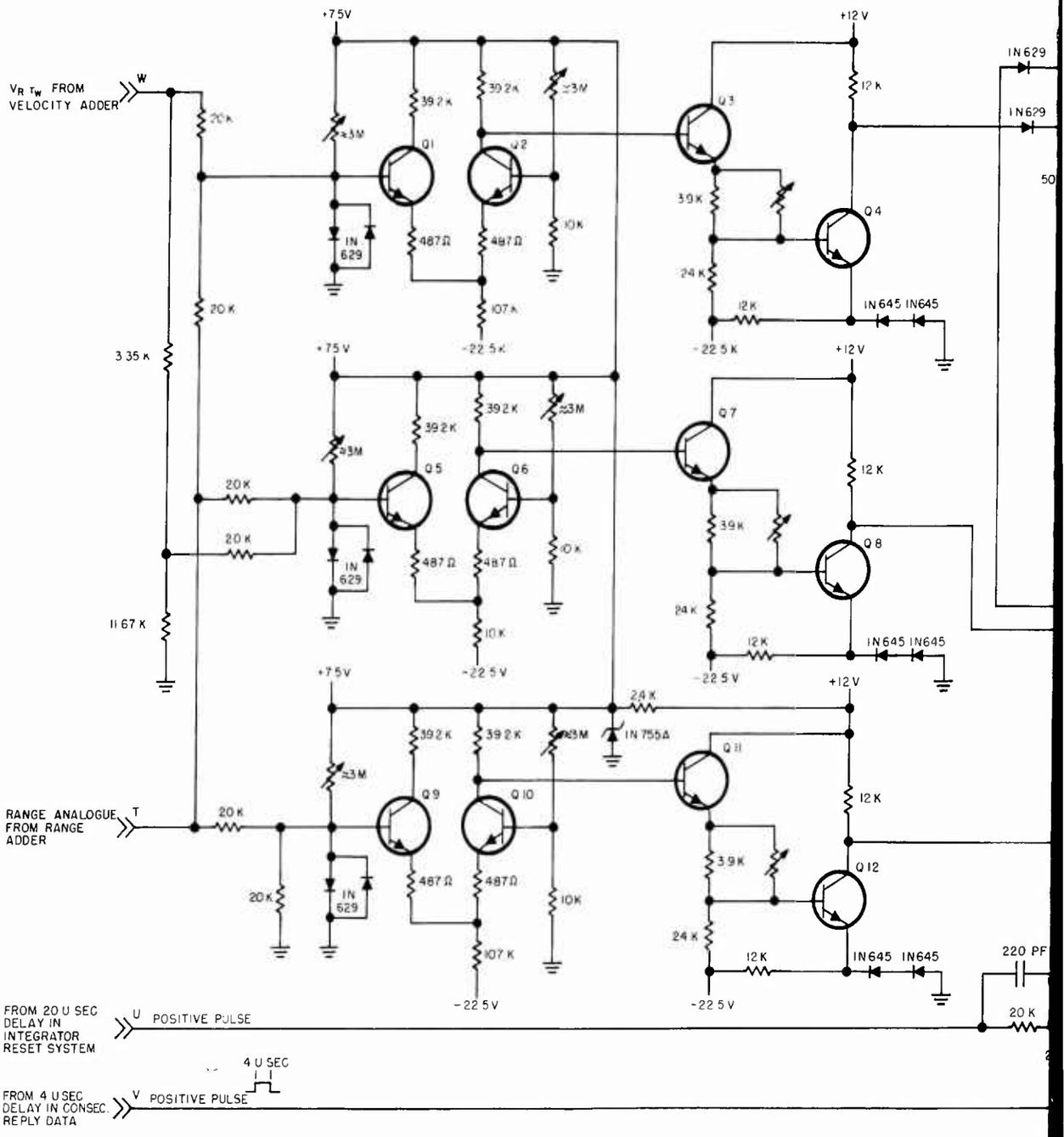
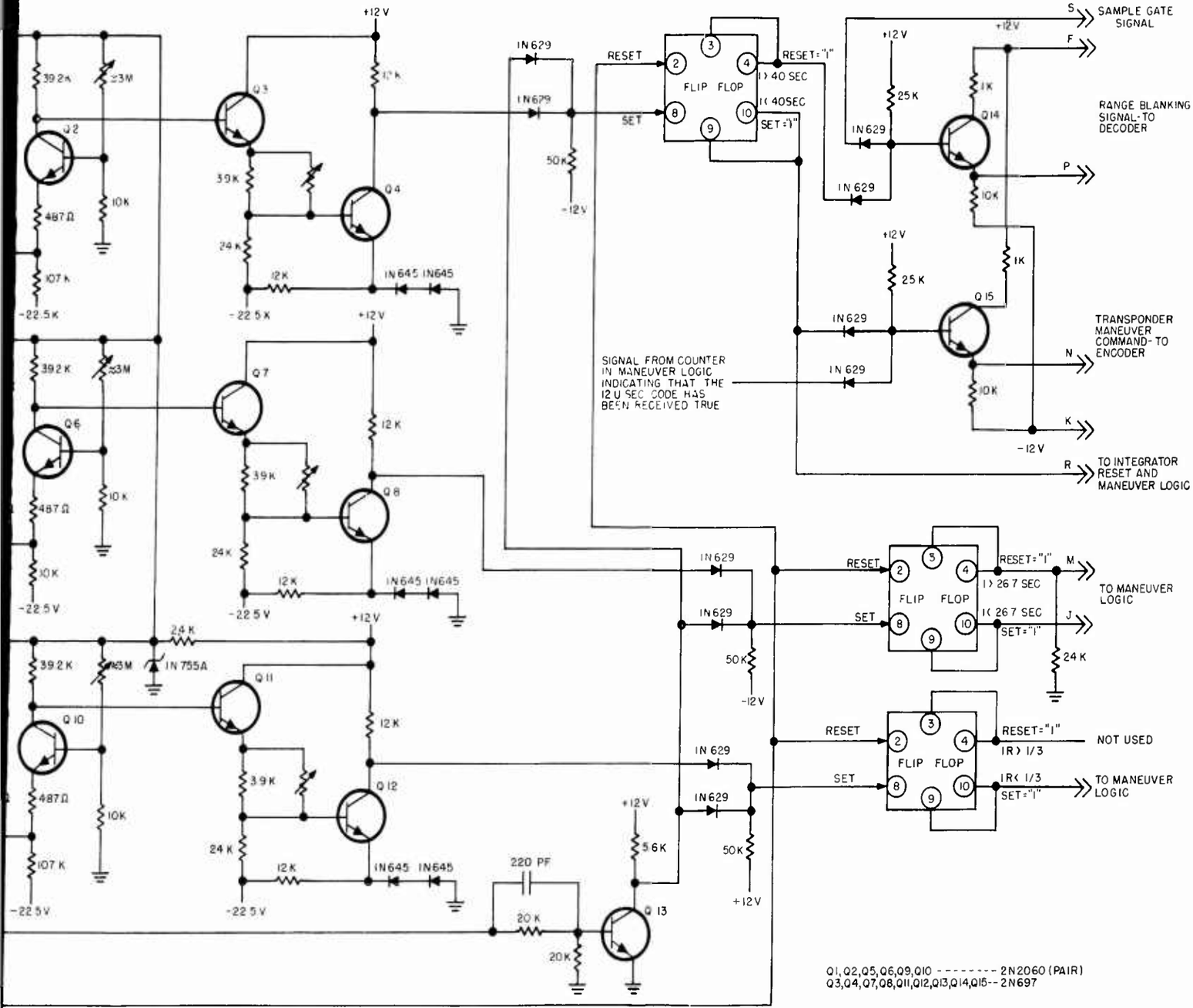


FIGURE 5-48. A-11 POWER AMPLIFIER INVERTING (INTERROGATOR)

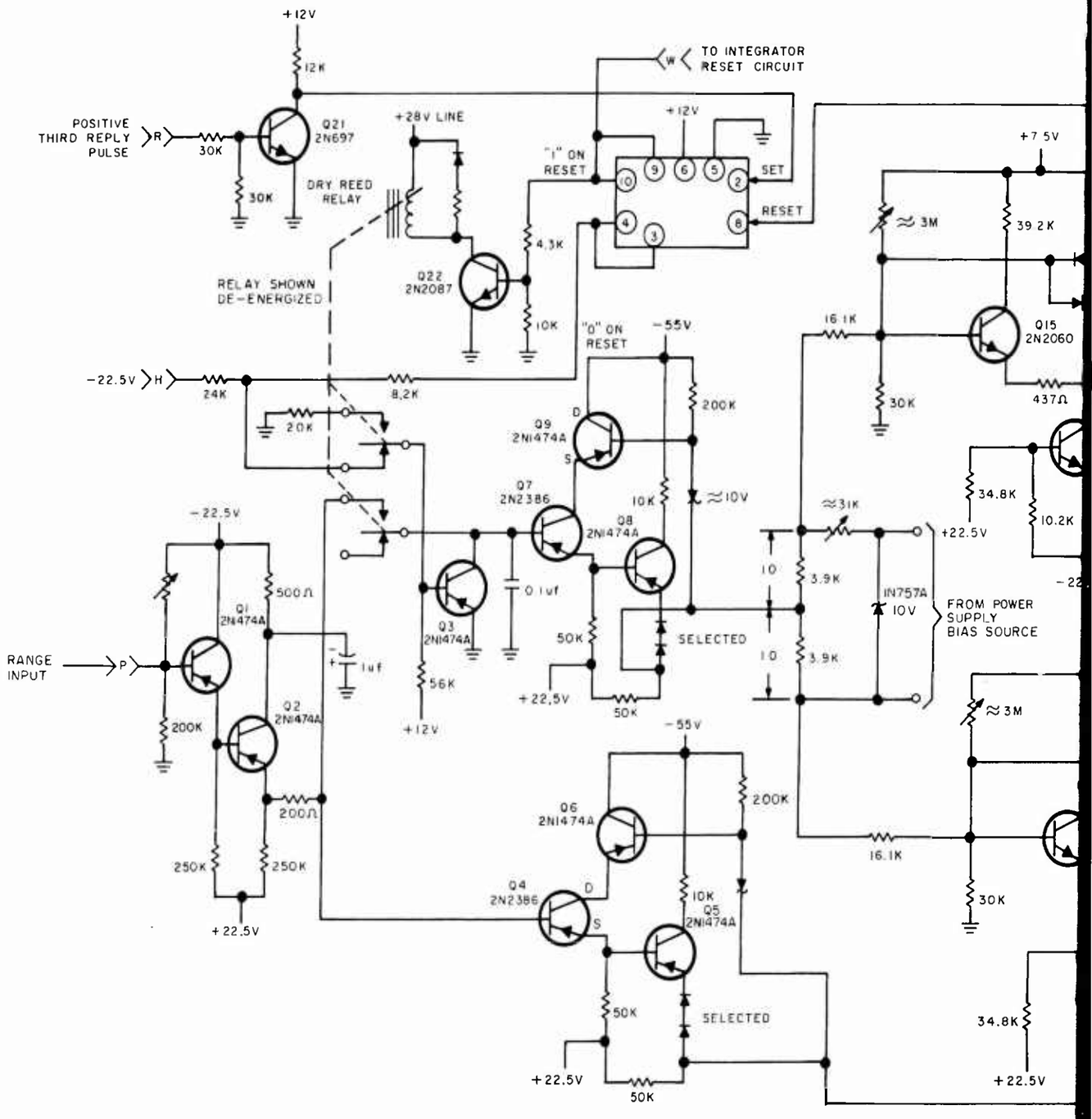

+75V
+12V
$V_R \tau_W$ FROM VELOCITY ADDER
W
20K
≈3M
392K
Q1
Q2
Q3
IN 629
487Ω
10K
107K
-22.5K
39K
Q4
24K
12K
IN645 IN645
IN629
IN629
50
3.35K
Q5
Q6
Q7
Q8
11.67K
Q9
Q10
Q11
Q12
24K
IN 755A
RANGE ANALOGUE FROM RANGE ADDER
T
FROM 20 U SEC DELAY IN INTEGRATOR RESET SYSTEM
U POSITIVE PULSE
4 U SEC
FROM 4 U SEC DELAY IN CONSEC. REPLY DATA
V POSITIVE PULSE
220 PF
20K



2

FIGURE 5-49

A-12 RANGE CRITERION COMPARATORS


+12V
12K
TO INTEGRATOR RESET CIRCUIT
W
POSITIVE THIRD REPLY PULSE
R
30K
Q21 2N697
30K
DRY REED RELAY
+28V LINE
"1" ON RESET
+12V
SET
RESET
4.3K
Q22 2N2087
10K
RELAY SHOWN DE-ENERGIZED
"0" ON RESET
-55V
-22.5V
H
24K
8.2K
20K
200K
Q9 2N1474A
Q7 2N2386
Q8 2N1474A
10K
≈10V
-22.5V
500Ω
Q1 2N1474A
0.1uf
Q3 2N1474A
50K
SELECTED
RANGE INPUT
P
1uf
56K
+12V
+22.5V
50K
200K
Q2 2N1474A
200Ω
250K
250K
+22.5V
-55V
Q6 2N1474A
200K
Q4 2N2386
10K
Q5 2N1474A
50K
SELECTED
+22.5V
50K
≈31K
+22.5V
10
3.9K
IN757A 10V
FROM POWER SUPPLY BIAS SOURCE
10
3.9K
+7.5V
≈3M
39.2K
16.1K
Q15 2N2060
30K
437Ω
34.8K
10.2K
≈3M
16.1K
30K
34.8K
+22.5V


1

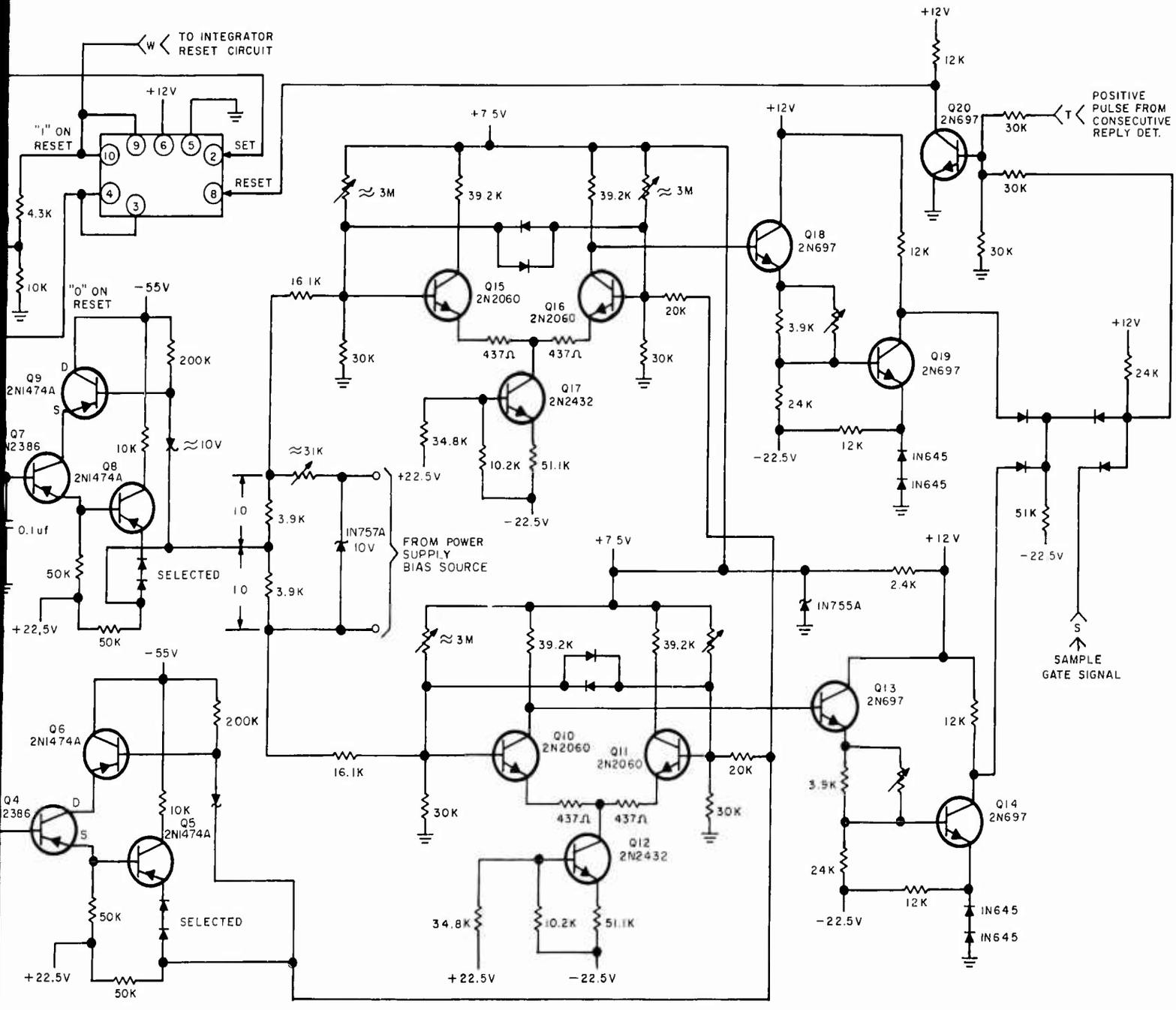
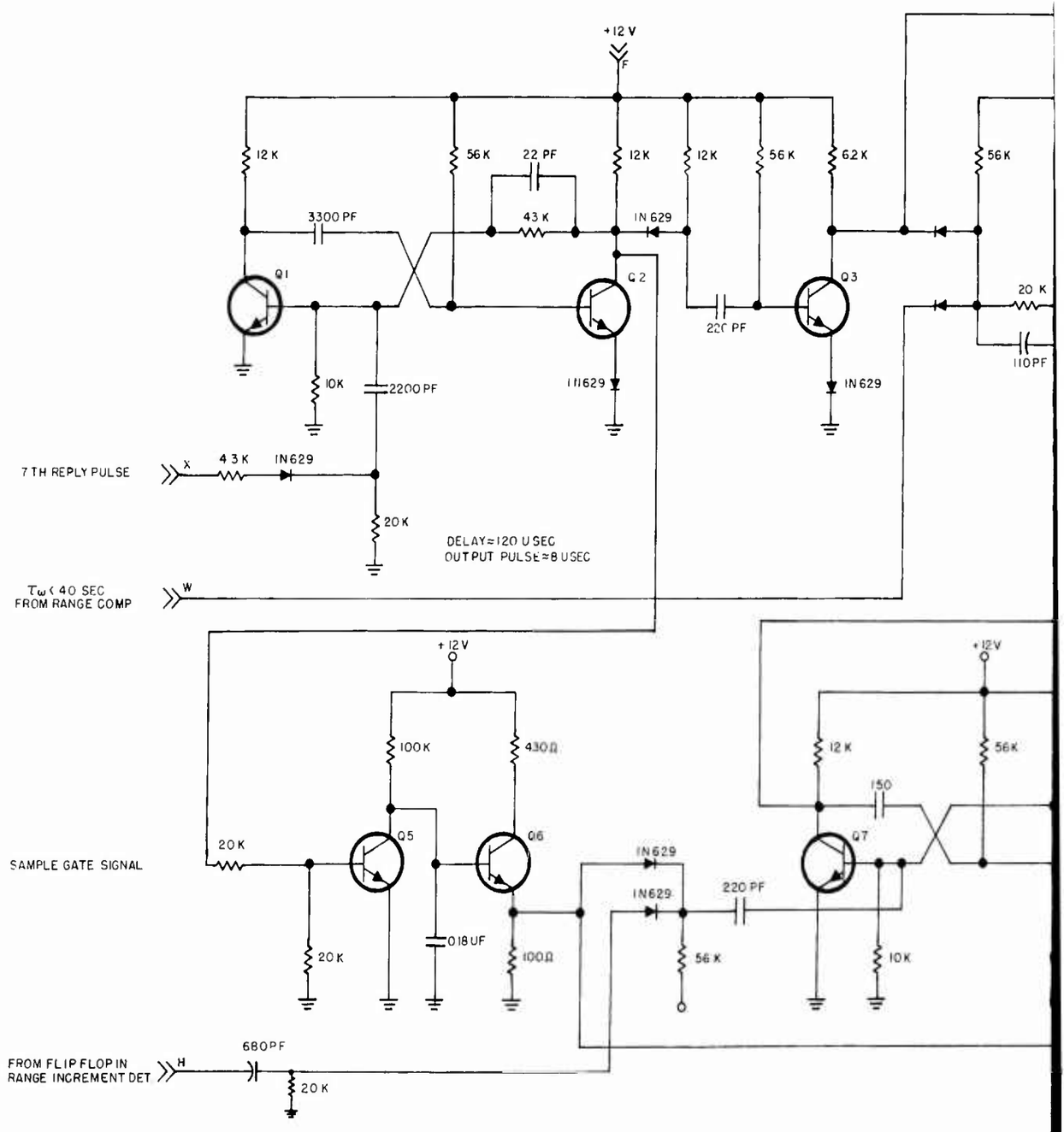


FIGURE 5-50

A-13 RANGE INCREMENT DETECTOR

2


+12 V
F
12 K
56 K
22 PF
12 K
12 K
56 K
62 K
56 K
3300 PF
43 K
IN 629
Q1
Q2
Q3
20 K
220 PF
110PF
10K
2200 PF
IN629
IN629
7TH REPLY PULSE
X
43 K
IN629
20 K
DELAY≈120 USEC
OUTPUT PULSE≈8 USEC
Tω (40 SEC
FROM RANGE COMP
W
+12 V
100 K
430Ω
20 K
Q5
Q6
SAMPLE GATE SIGNAL
20 K
.018 UF
100Ω
IN629
IN629
220 PF
56 K
+12V
12 K
56K
150
Q7
10K
680PF
FROM FLIP FLOP IN
RANGE INCREMENT DET
H
20 K

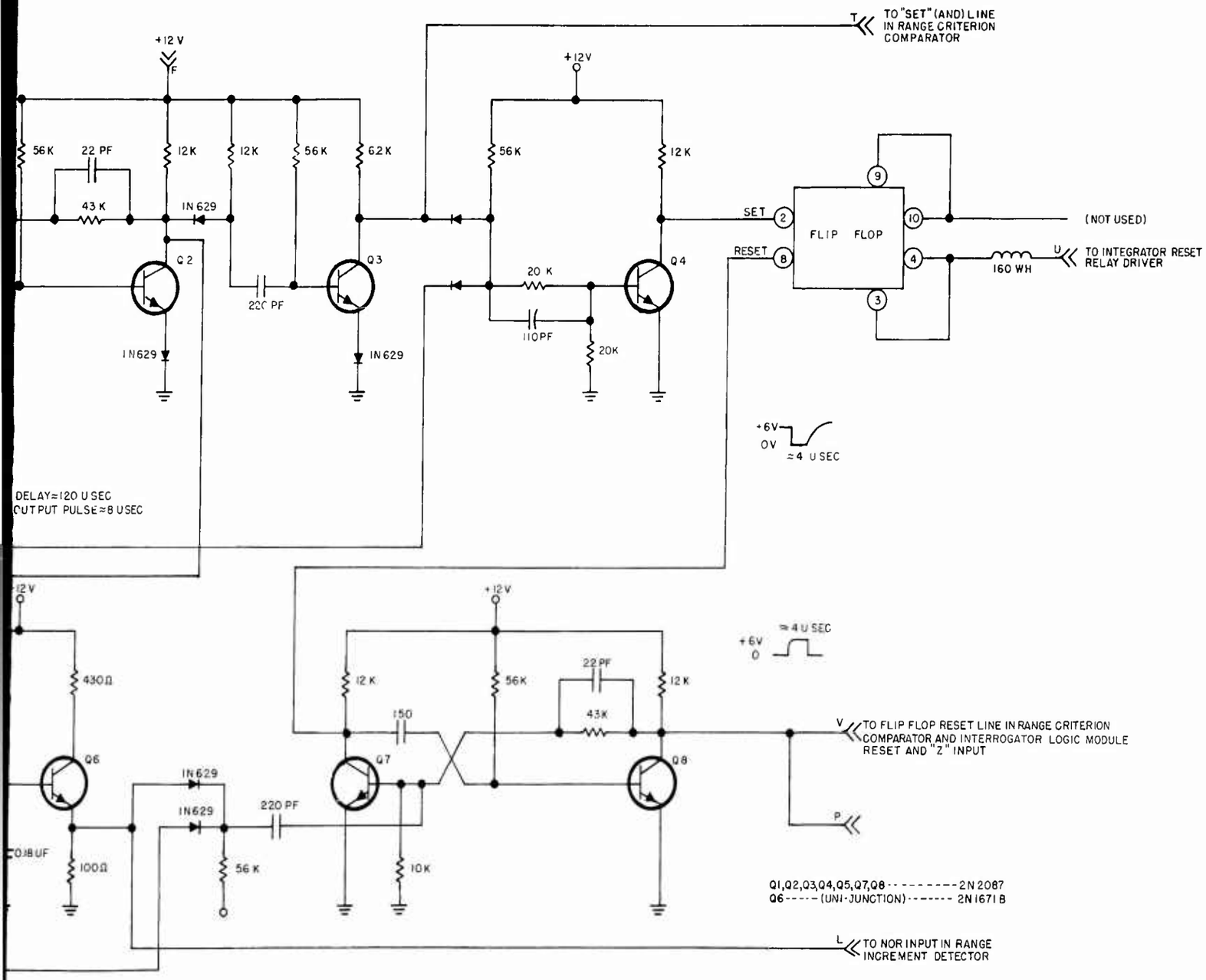
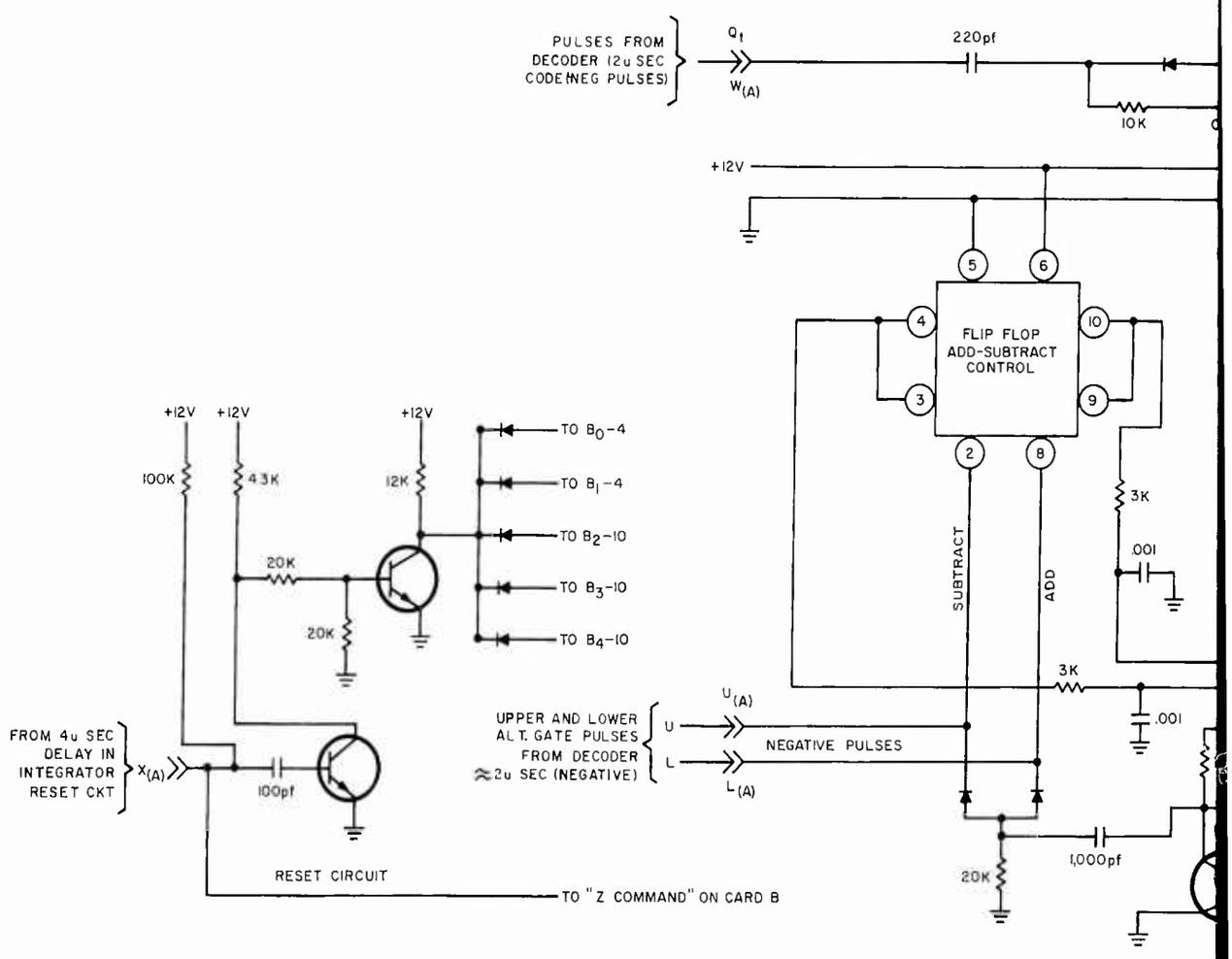


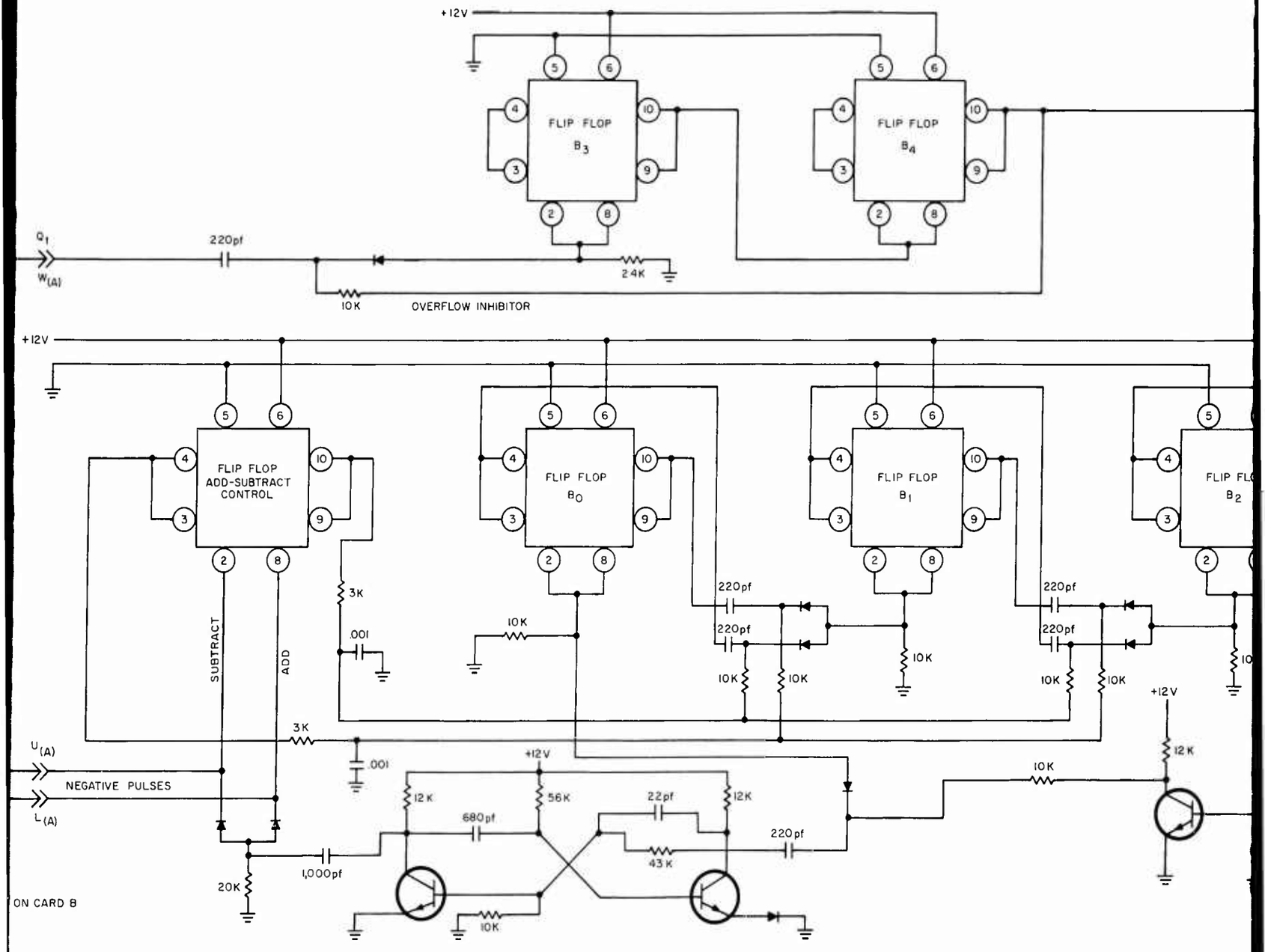
FIGURE 5-51

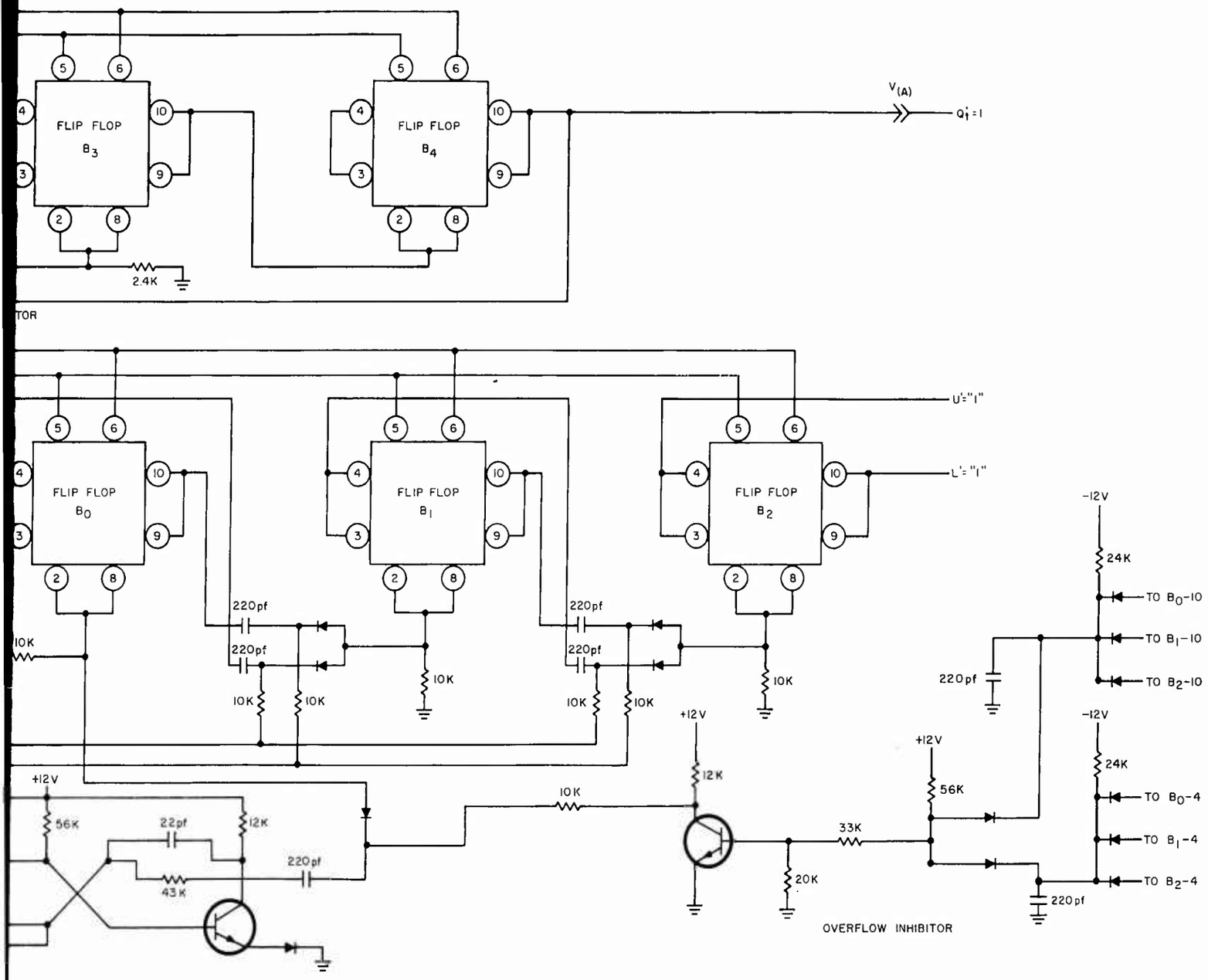
A-14 INTEGRATOR RESET AND CONSECUTIVE REPLY DETECTOR

2


PULSES FROM DECODER 12u SEC CODE (NEG PULSES)
Q_1
$W_{(A)}$
220pf
10K
+12V
5
6
4
10
3
9
2
8
FLIP FLOP ADD-SUBTRACT CONTROL
SUBTRACT
ADD
3K
.001
3K
.001
+12V
+12V
+12V
100K
43K
12K
20K
20K
TO B_0-4
TO B_1-4
TO B_2-10
TO B_3-10
TO B_4-10
FROM 4u SEC DELAY IN INTEGRATOR RESET CKT
$X_{(A)}$
100pf
UPPER AND LOWER ALT. GATE PULSES FROM DECODER ≈2u SEC (NEGATIVE)
U
L
$U_{(A)}$
$L_{(A)}$
NEGATIVE PULSES
20K
1,000pf
RESET CIRCUIT
TO "Z COMMAND" ON CARD B

1

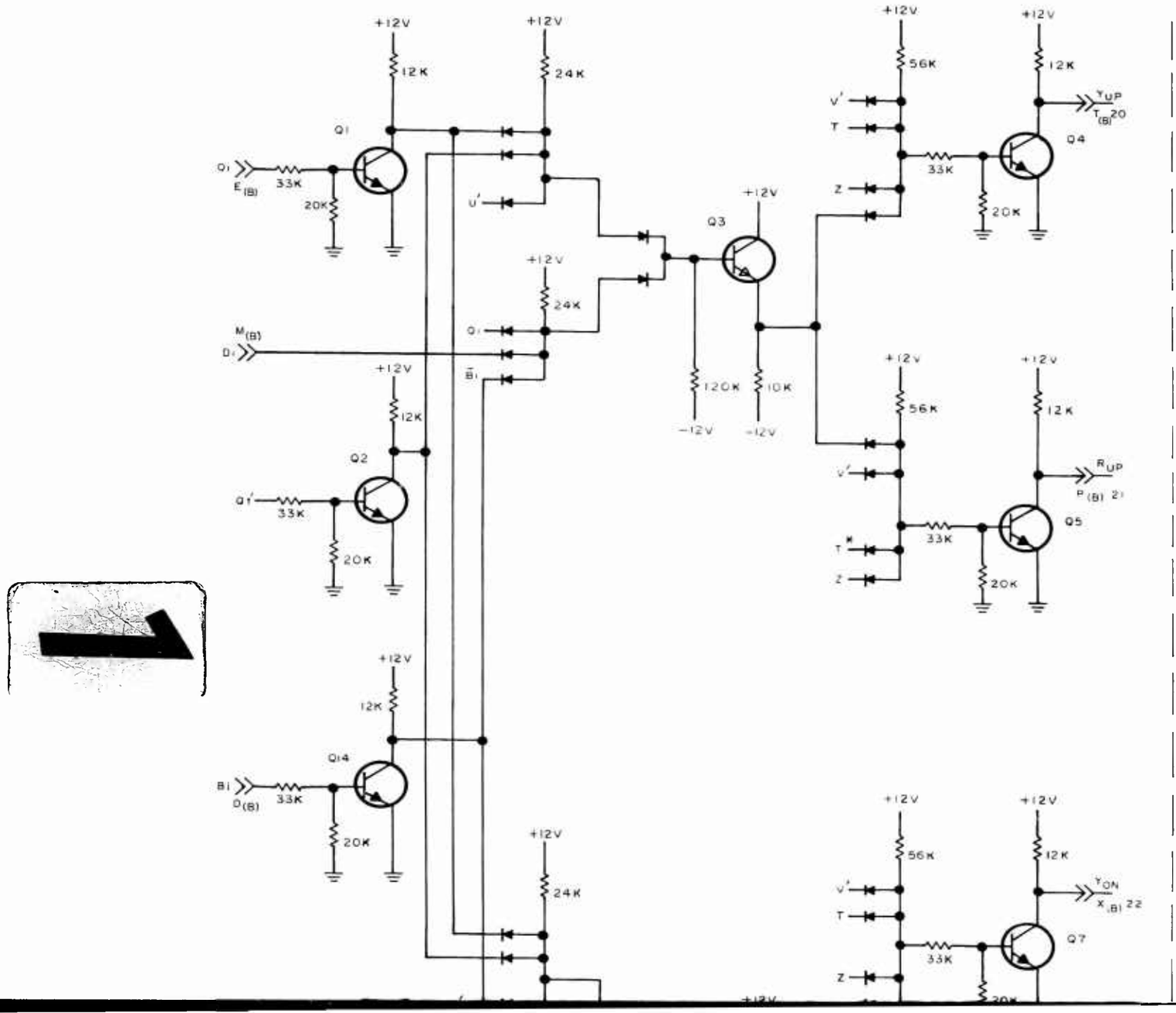

+12V
FLIP FLOP
B3
FLIP FLOP
B4
Q1
W(A)
220pf
24K
10K
OVERFLOW INHIBITOR
+12V
FLIP FLOP
ADD-SUBTRACT
CONTROL
FLIP FLOP
B0
FLIP FLOP
B1
FLIP FLOP
B2
3K
.001
10K
220pf
SUBTRACT
ADD
U(A)
NEGATIVE PULSES
L(A)
3K
.001
+12V
12K
56K
680pf
22pf
12K
220pf
43K
20K
1,000pf
10K
ON CARD B
10K
+12V
12K



3

FIGURE 5-52

A-15 INTERROGATOR MANEUVER LOGIC (SHEET 1 OF 2)


+12V
12K
24K
Q1
Q1 E(B)
33K
20K
U'
+12V
Q3
120K
10K
-12V
-12V
+12V
24K
Q1
M(B) D1
B1
+12V
12K
Q2
Q1'
33K
20K
+12V
56K
V'
T
Z
33K
20K
+12V
12K
YUP T(B)20
Q4
+12V
56K
V'
T
M
Z
33K
20K
+12V
12K
RUP P(B) 21
Q5
+12V
12K
Q14
B1 D(B)
33K
20K
+12V
24K
+12V
56K
V'
T
Z
33K
20K
+12V
12K
YON X(B) 22
Q7

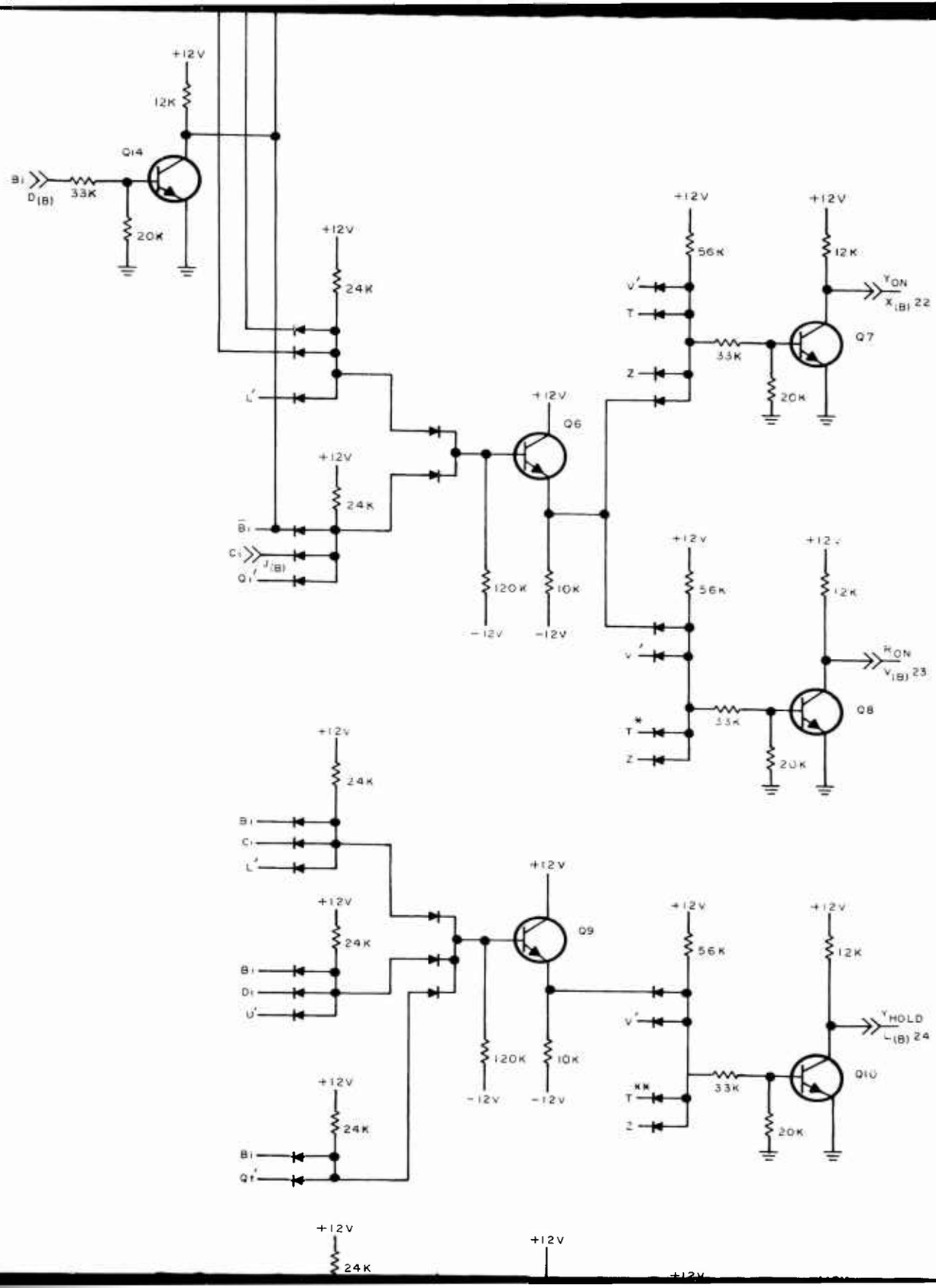

+12V
12K
Q14
B1
D(B)
33K
20K
24K
L'
B1
C1
Q1'
J(B)
120K
10K
-12V
Q6
56K
V'
T
Z
33K
20K
Q7
Y ON
X(B) 22
V'
T
Z
33K
20K
Q8
R ON
V(B) 23
B1
C1
L'
B1
D1
U'
B1
Q1'
Q9
56K
V'
KK
T
Z
33K
20K
Q10
Y HOLD
L(B) 24
TO SCAN MEMORY

FIGURE 5-52

A-15 INTERROGATOR MANEUVER LOGIC (SH

3

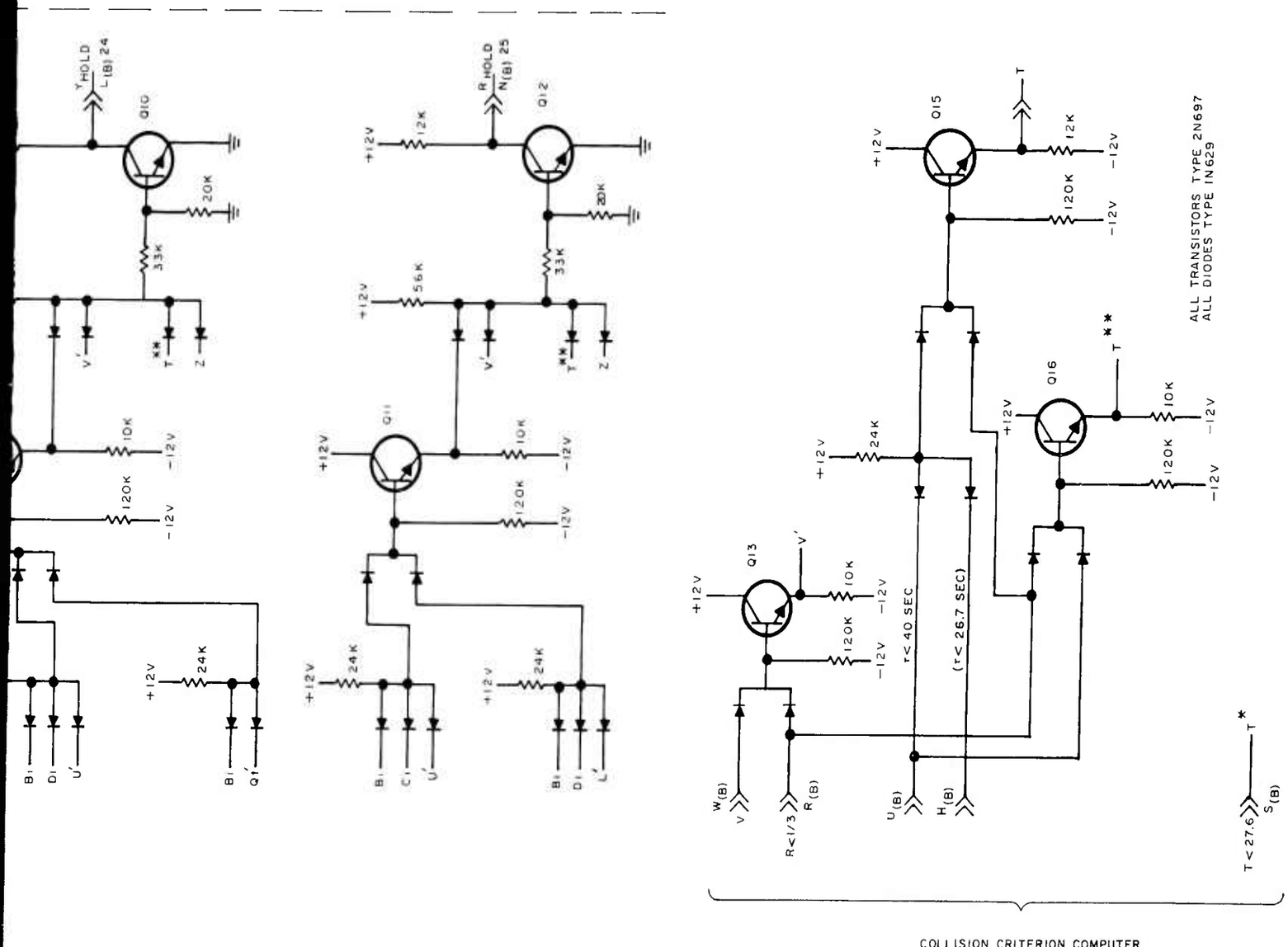
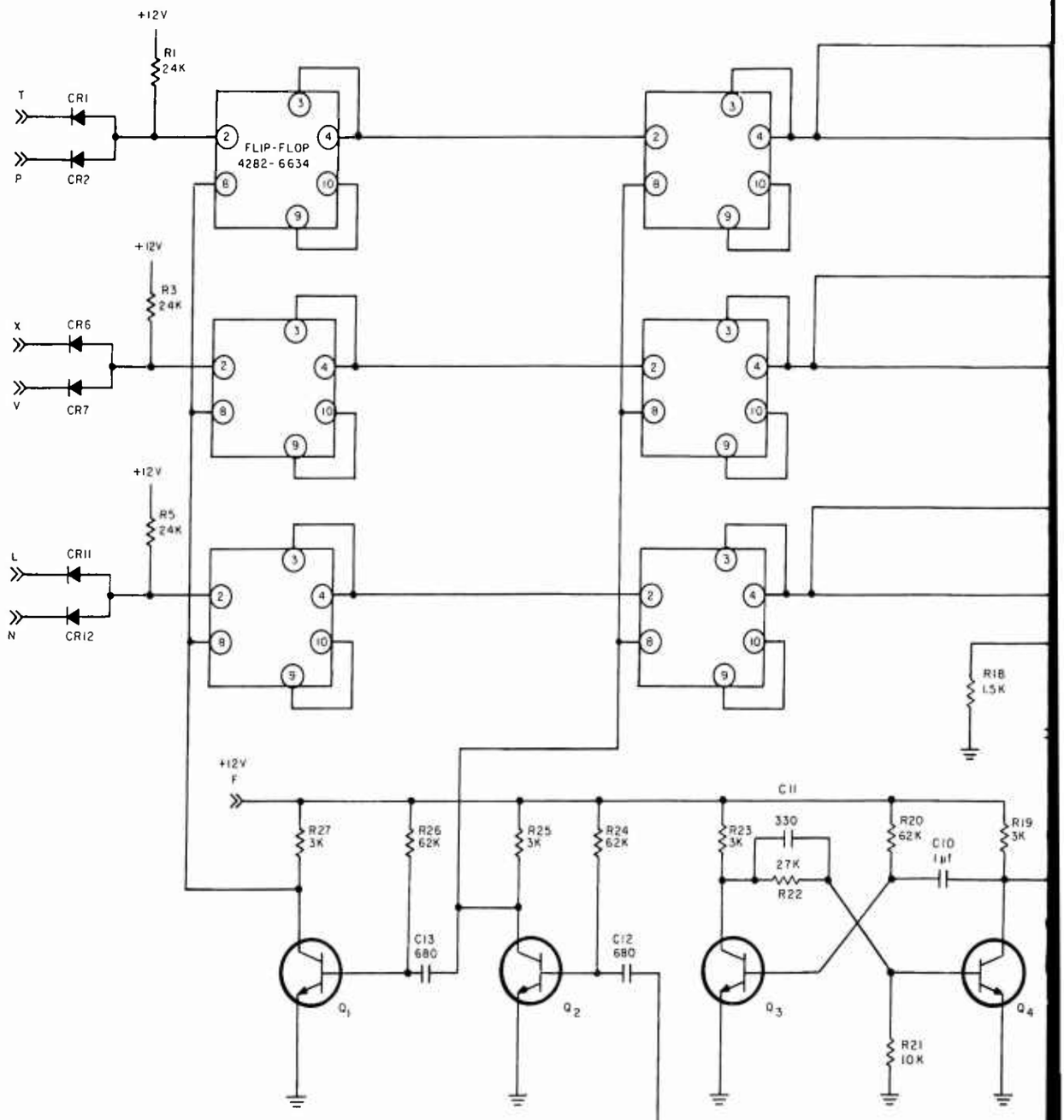


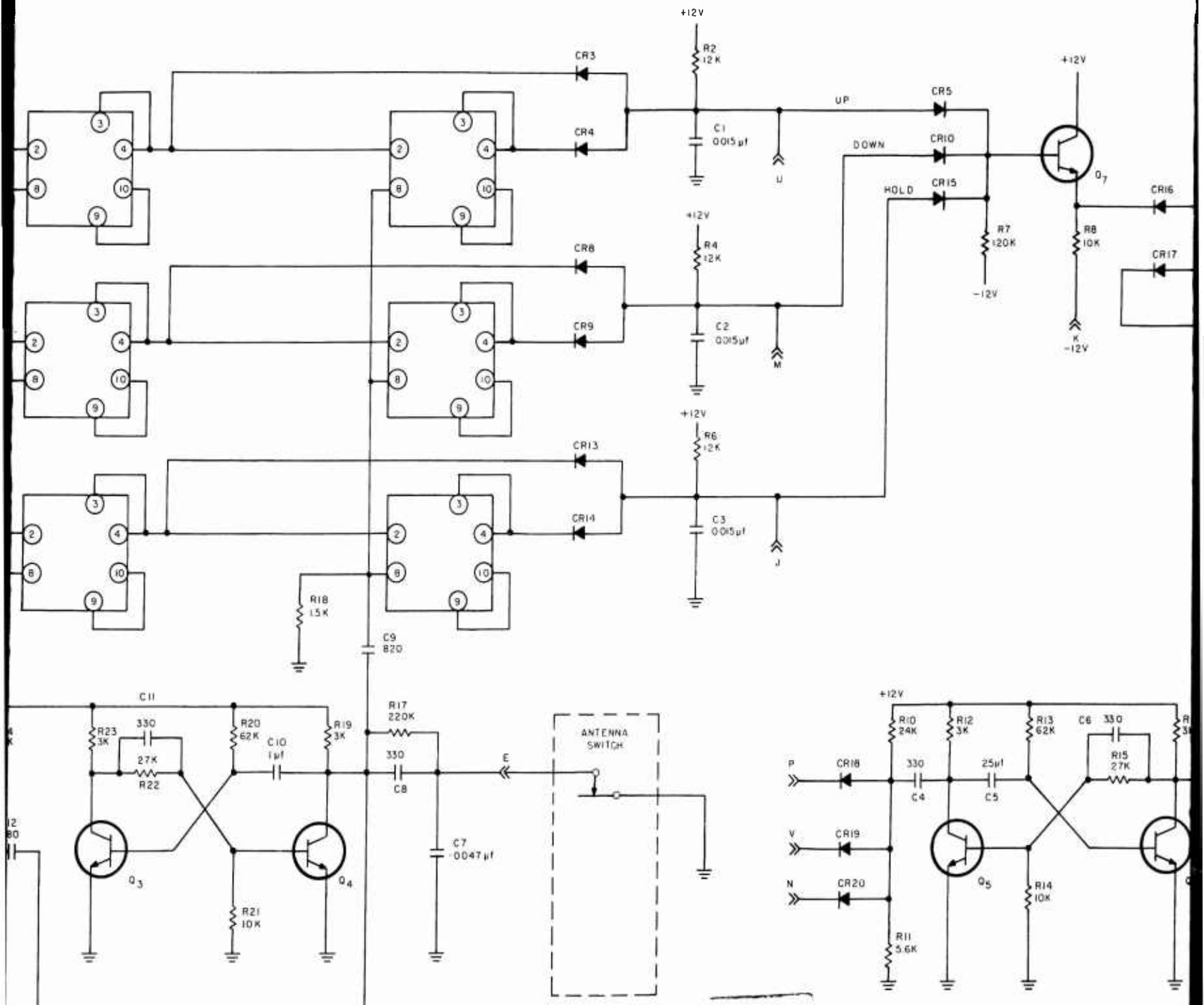
FIGURE 5-52

A-15 INTERROGATOR MANEUVER LOGIC (SHEET 2 OF 2)



ALL DIODES TYPE IN629
ALL TRANSISTORS TYPE 2N697
ALL CAPACITORS IN pf UNLESS OTHERWISE NOTED

1


+12V
R2 12K
CR3
CR4
C1 0.015 µf
U
UP
CR5
DOWN
CR10
HOLD
CR15
R7 120K
-12V
+12V
Q7
CR16
R8 10K
CR17
K
-12V
+12V
R4 12K
CR8
CR9
C2 0.015µf
M
+12V
R6 12K
CR13
CR14
C3 0.015µf
J
R18 1.5K
C9 820
C11
R23 3K
330
27K R22
R20 62K
C10 1µf
R19 3K
R17 220K
330 C8
E
ANTENNA SWITCH
C7 0.047 µf
Q3
Q4
R21 10K
+12V
R10 24K
R12 3K
R13 62K
C6 330
R15 27K
P
CR18
330 C4
25µf C5
V
CR19
N
CR20
Q5
R14 10K
R11 5.6K

2

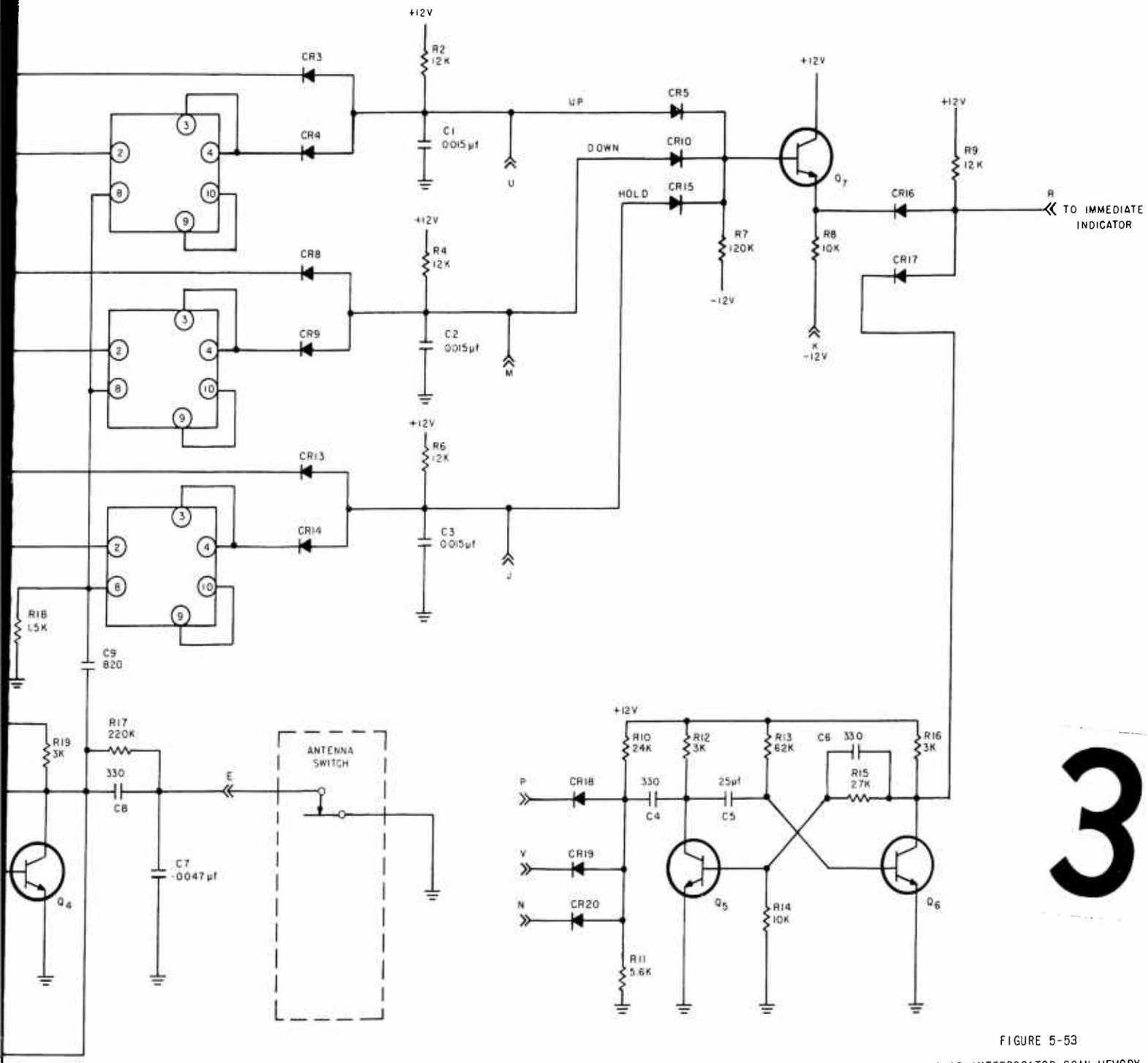


FIGURE 5-53

A-16 INTERROGATOR SCAN MEMORY

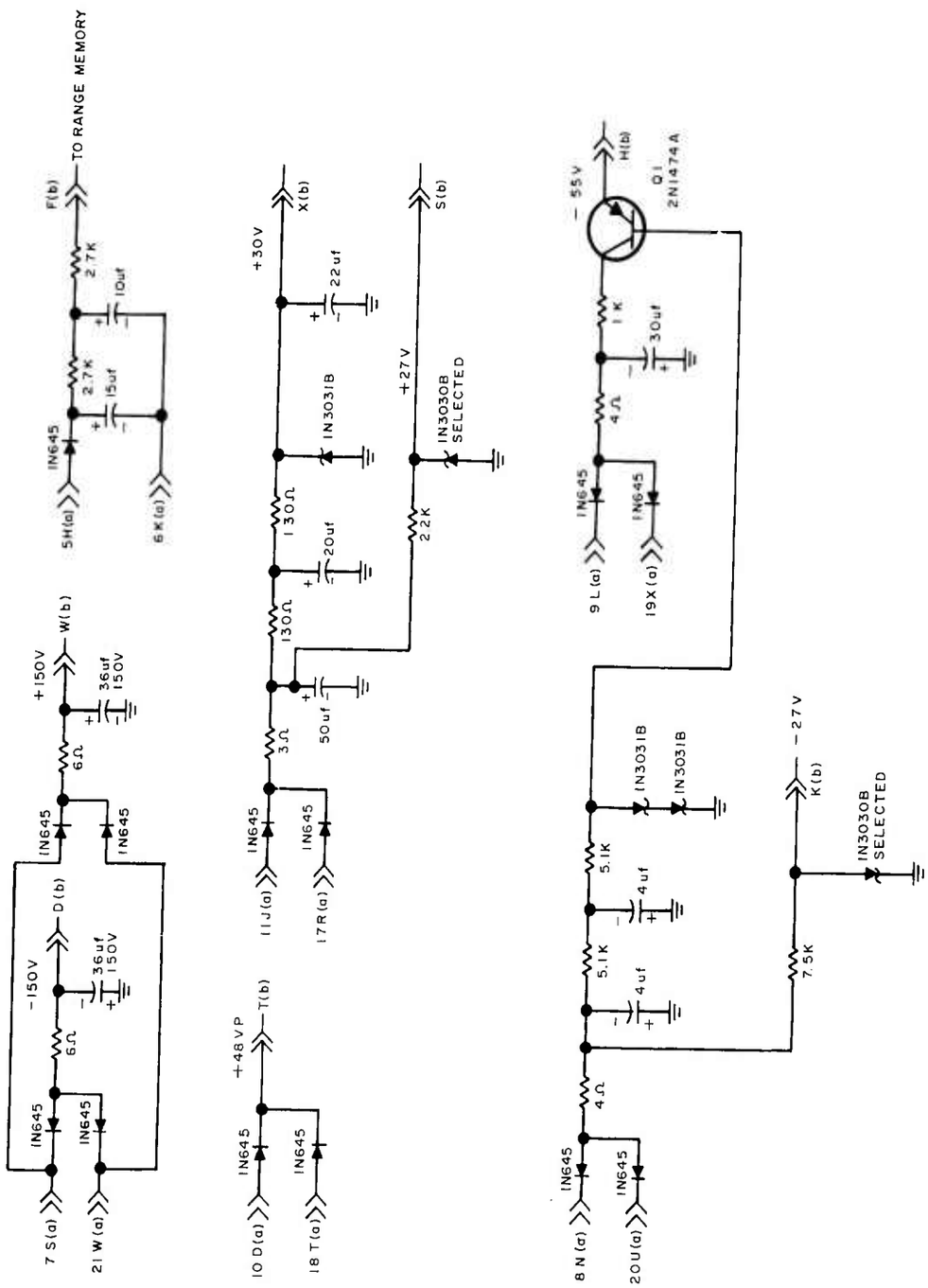


FIGURE 5-54. A-17 INTERROGATOR RECTIFIERS AND REGULATORS (SHEET 1 OF 3)

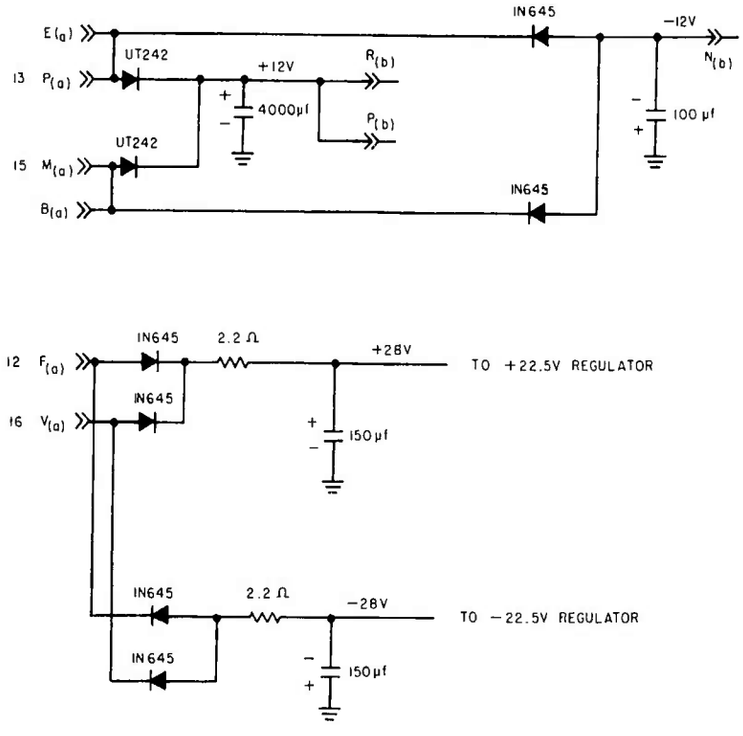
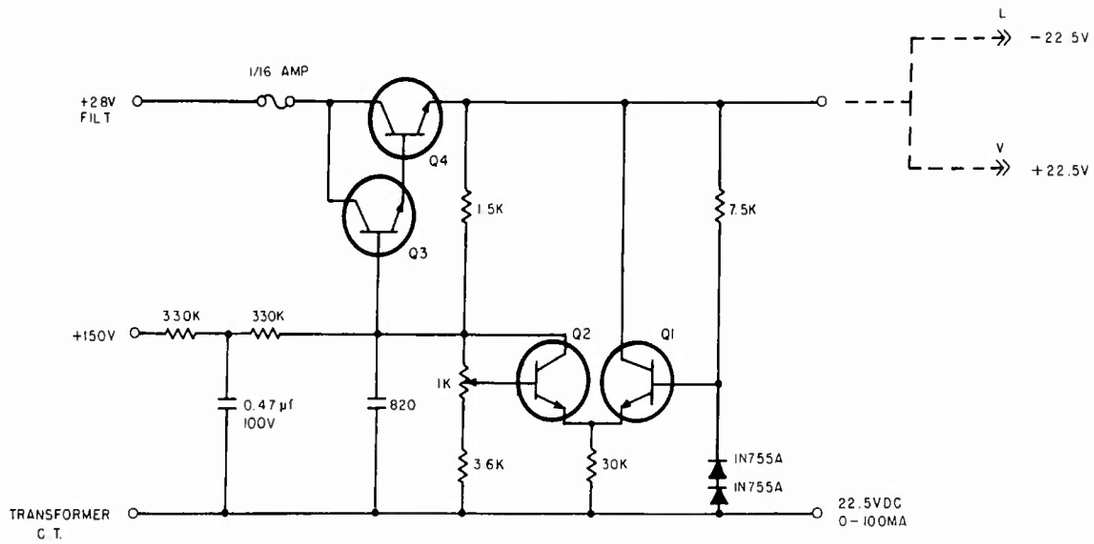


FIGURE 5-54. A-17 INTERROGATOR RECTIFIERS AND REGULATORS (SHEET 2 OF 3)



NOTE: FOR +22.5V SUPPLY THE TRANSISTORS TO BE USED ARE AS GIVEN BELOW AND THE CONNECTIONS ARE AS SHOWN ABOVE.

Q_1, Q_2 ——— 2N338

Q_3, Q_4 ——— 2N697

FOR THE -22.5V SUPPLY THE TRANSISTORS TO BE USED ARE AS GIVEN BELOW, THE DIODES ARE REVERSED AND THE UN-REGULATED SUPPLIES ARE -28V AND -150V

Q_1, Q_2, Q_3, Q_4 ——— 2N1474A

FIGURE 5-54. A-17 INTERROGATOR RECTIFIERS AND REGULATORS (SHEET 3 OF 3)

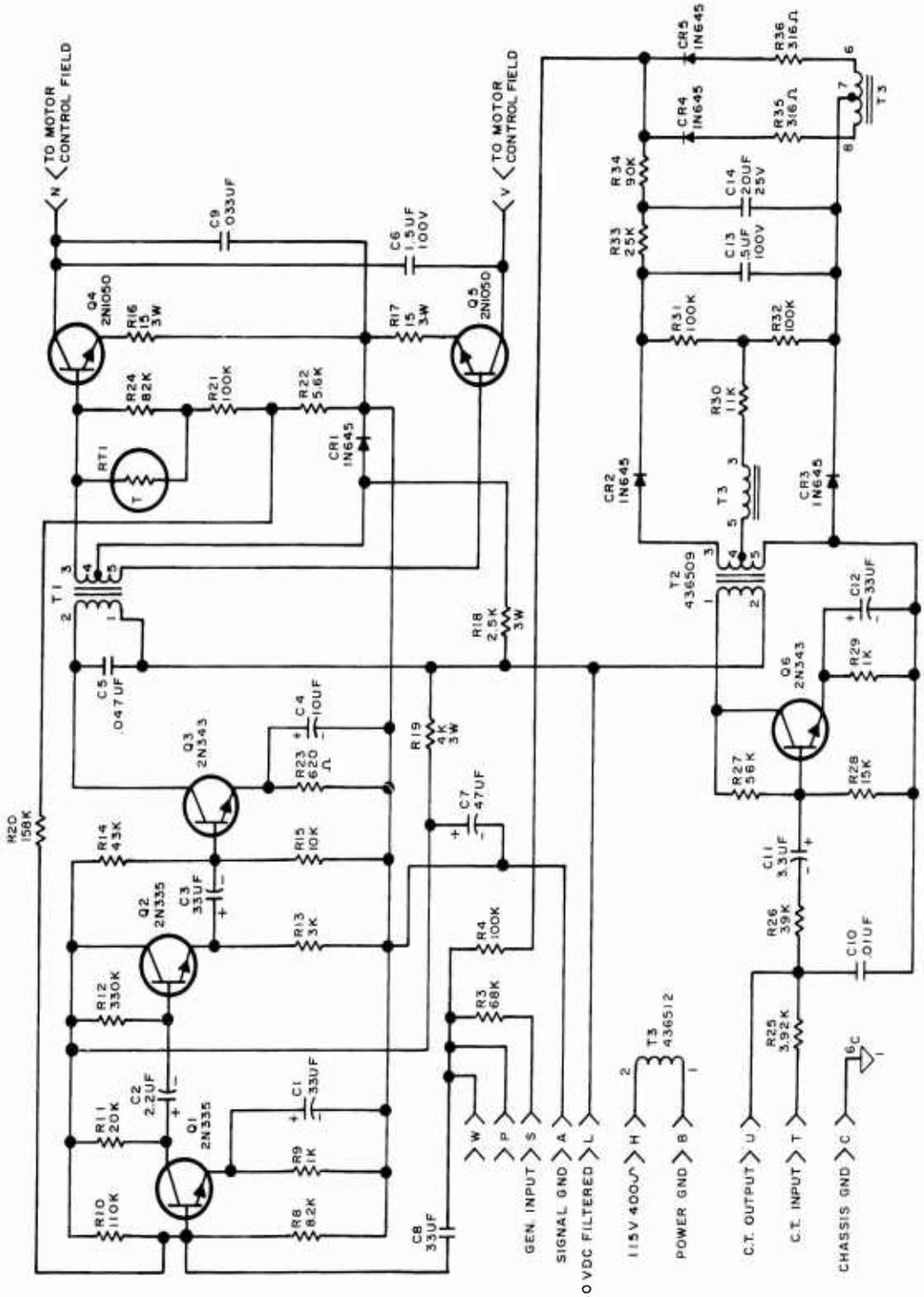


FIGURE 5-55. A-18 HEADING MOTOR AMPLIFIER (3)

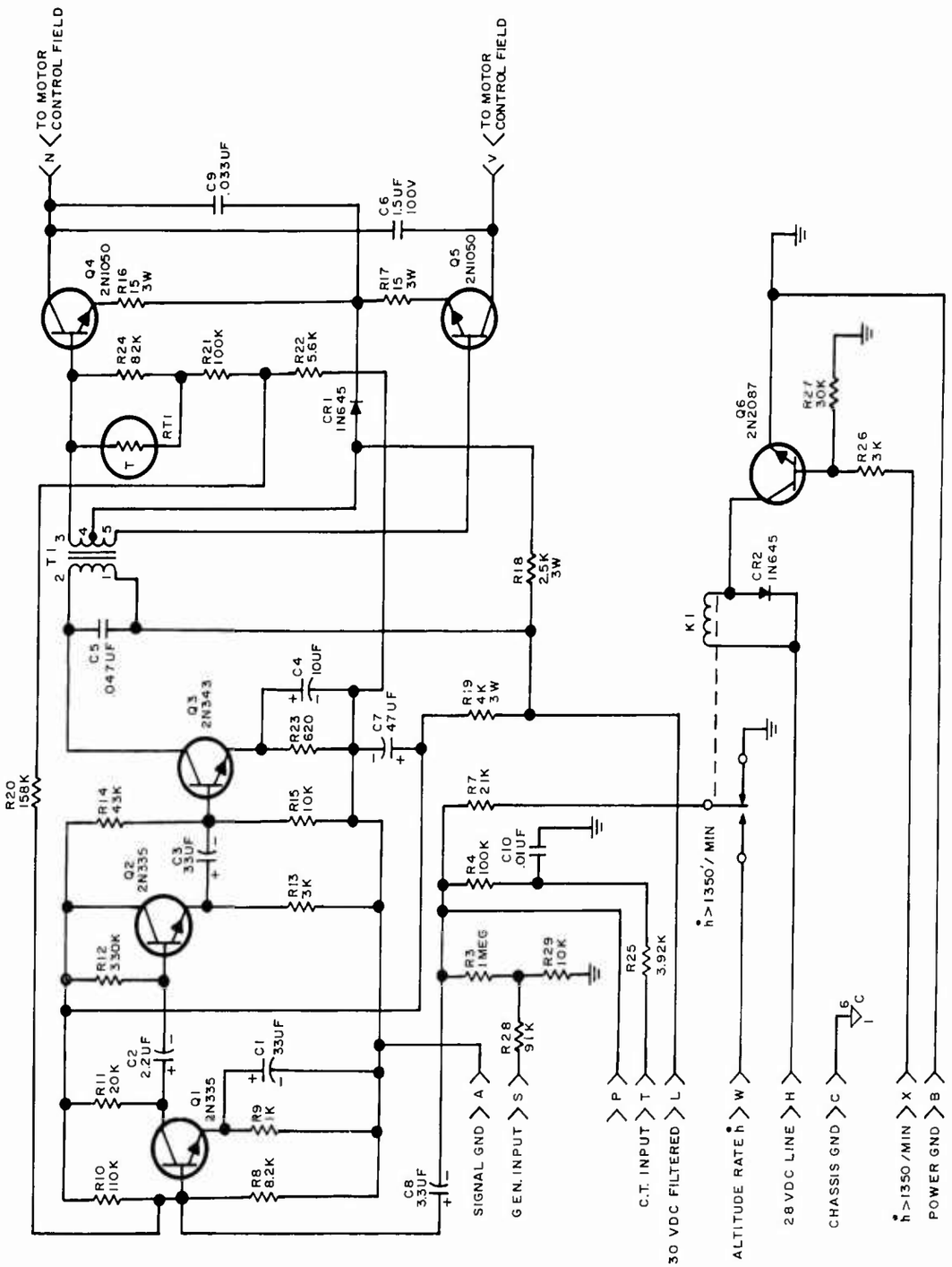


FIGURE 5-56. A-19 ALTITUDE MOTOR AMPLIFIER (h)

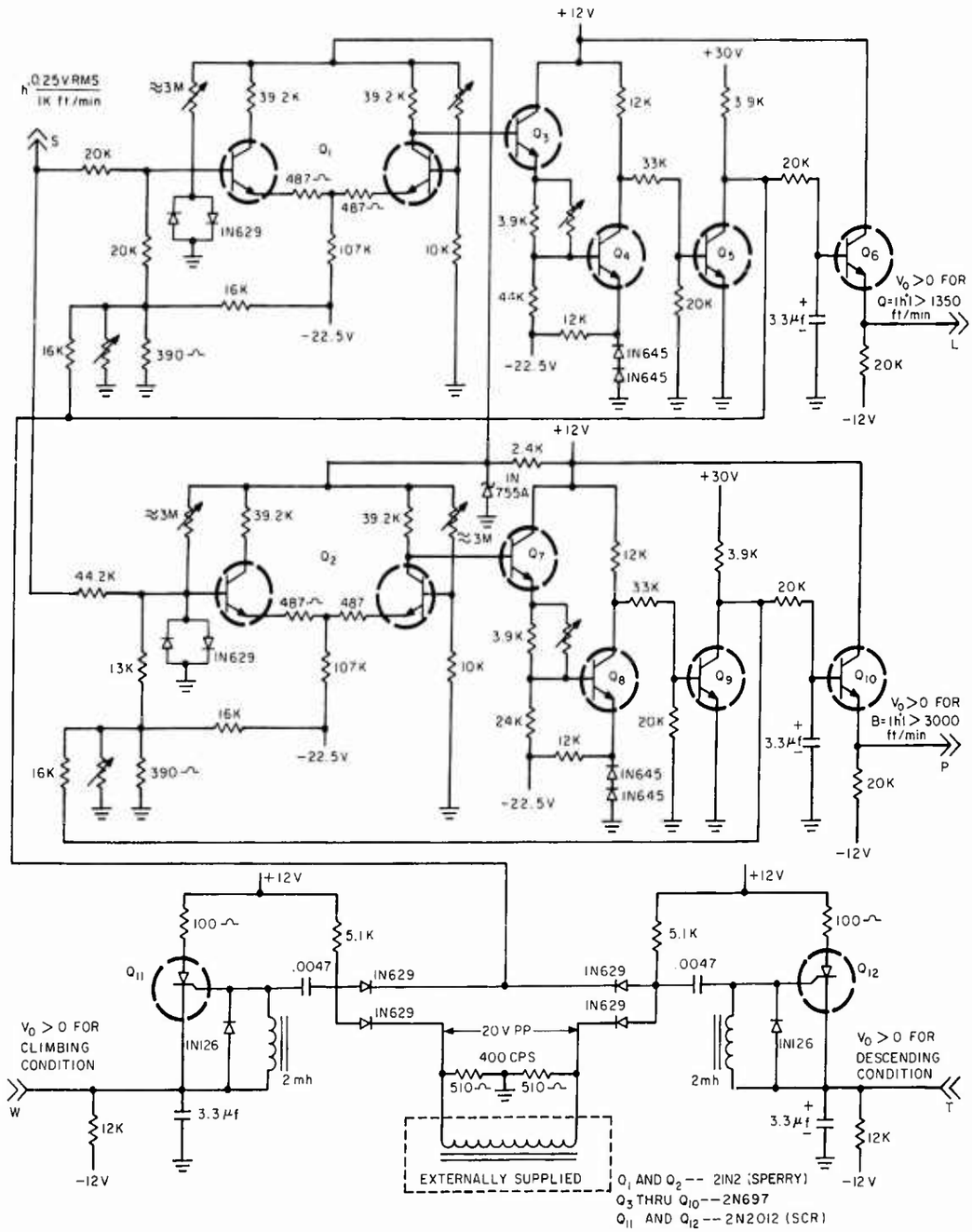
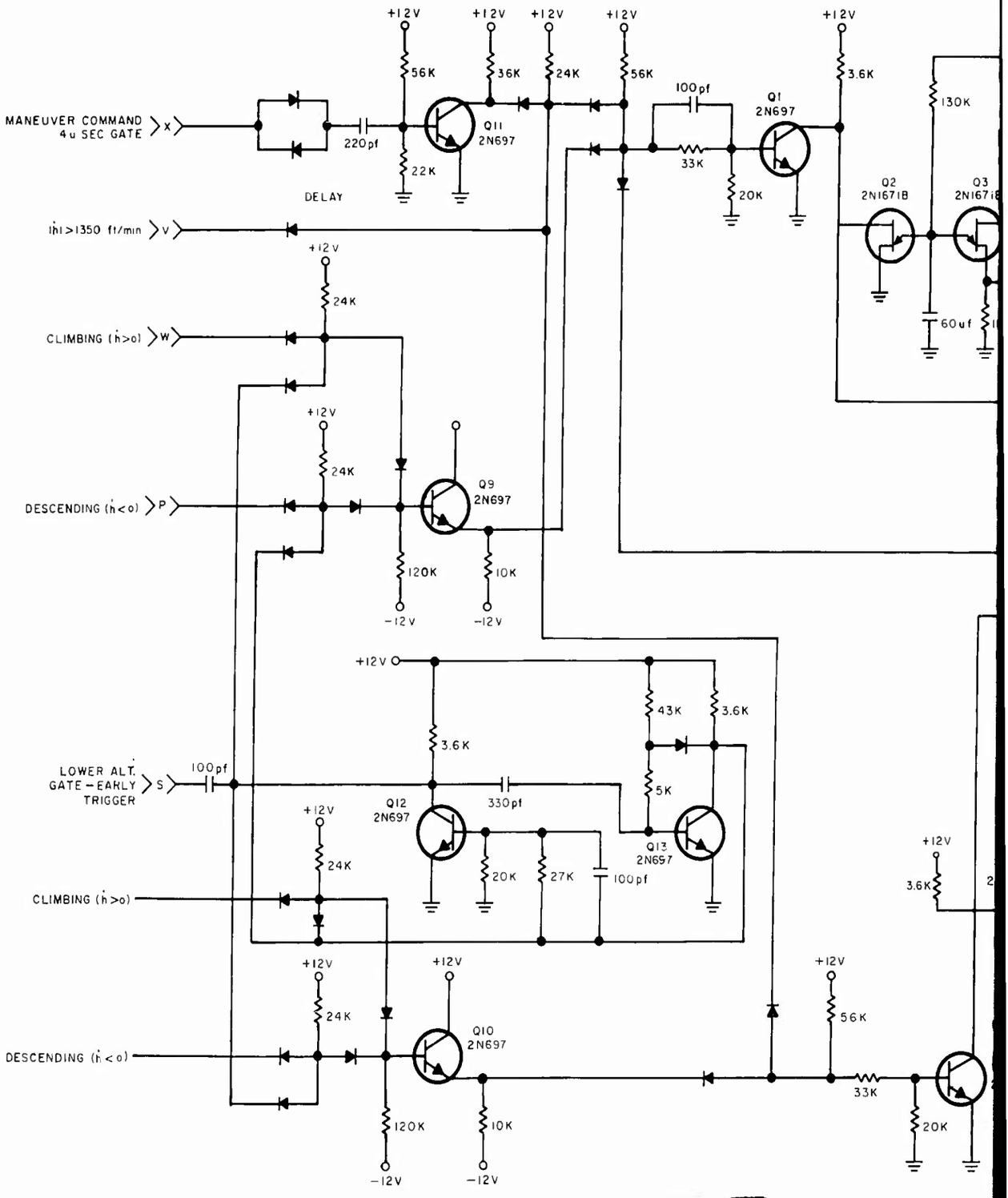


FIGURE 5-57

A-20 CLIMB RATE DETECTOR


MANEUVER COMMAND
4u SEC GATE
X
DELAY
|ḣ|>1350 ft/min
V
CLIMBING (ḣ>o)
W
DESCENDING (ḣ<o)
P
LOWER ALT.
GATE – EARLY
TRIGGER
S
CLIMBING (ḣ>o)
DESCENDING (ḣ<o)
+12V
-12V
56K
36K
24K
22K
220pf
Q11
2N697
100pf
33K
20K
Q1
2N697
3.6K
130K
Q2
2N1671B
Q3
2N167
60uf
Q9
2N697
120K
10K
43K
5K
330pf
Q12
2N697
Q13
2N697
27K
Q10
2N697

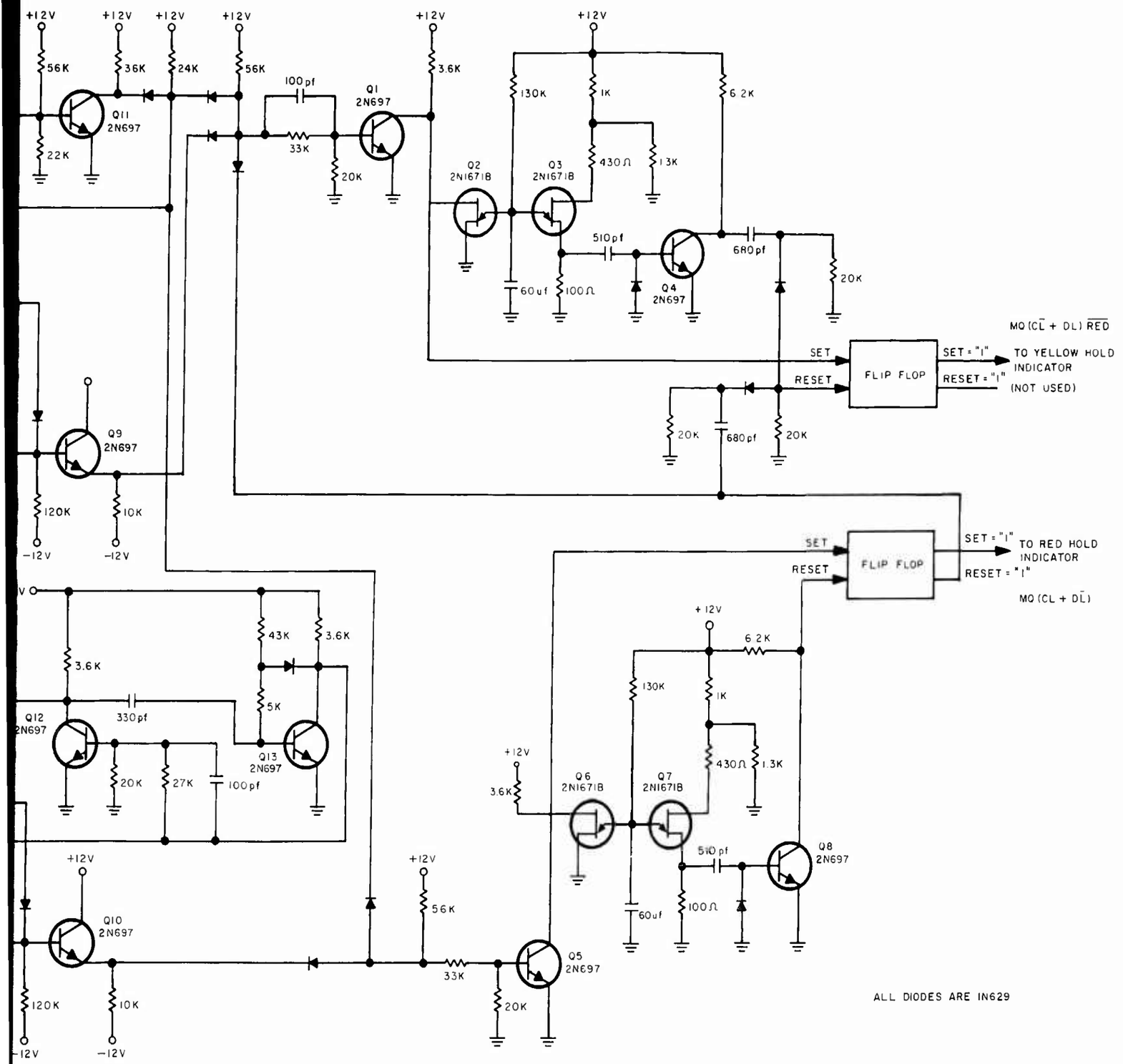


FIGURE 5-58

A-21 TRANSPONDER MANEUVER LOGIC

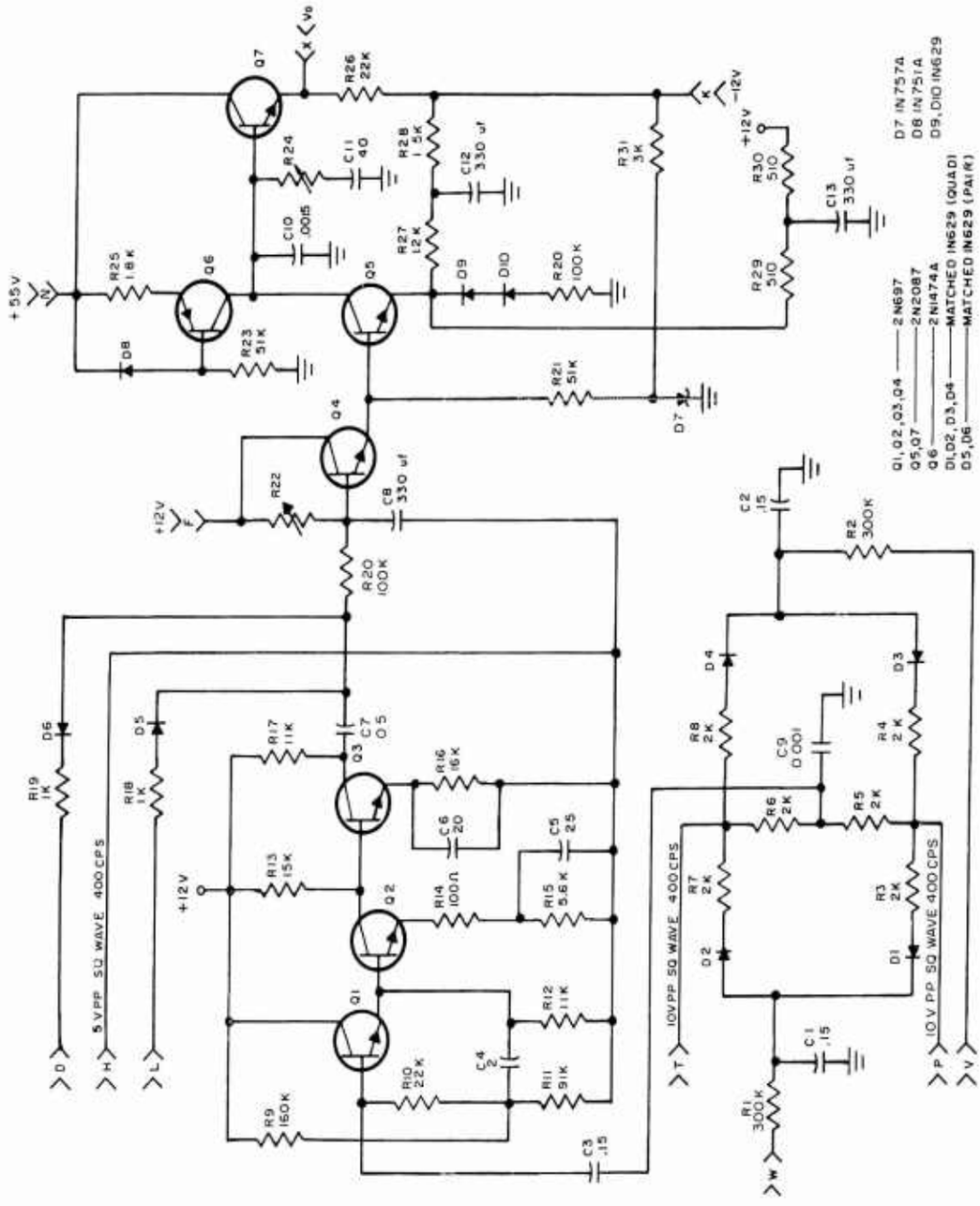


FIGURE 5-59. A-22 POWER AMPLIFIER (NON-INVERTING) (TRANSPONDER)

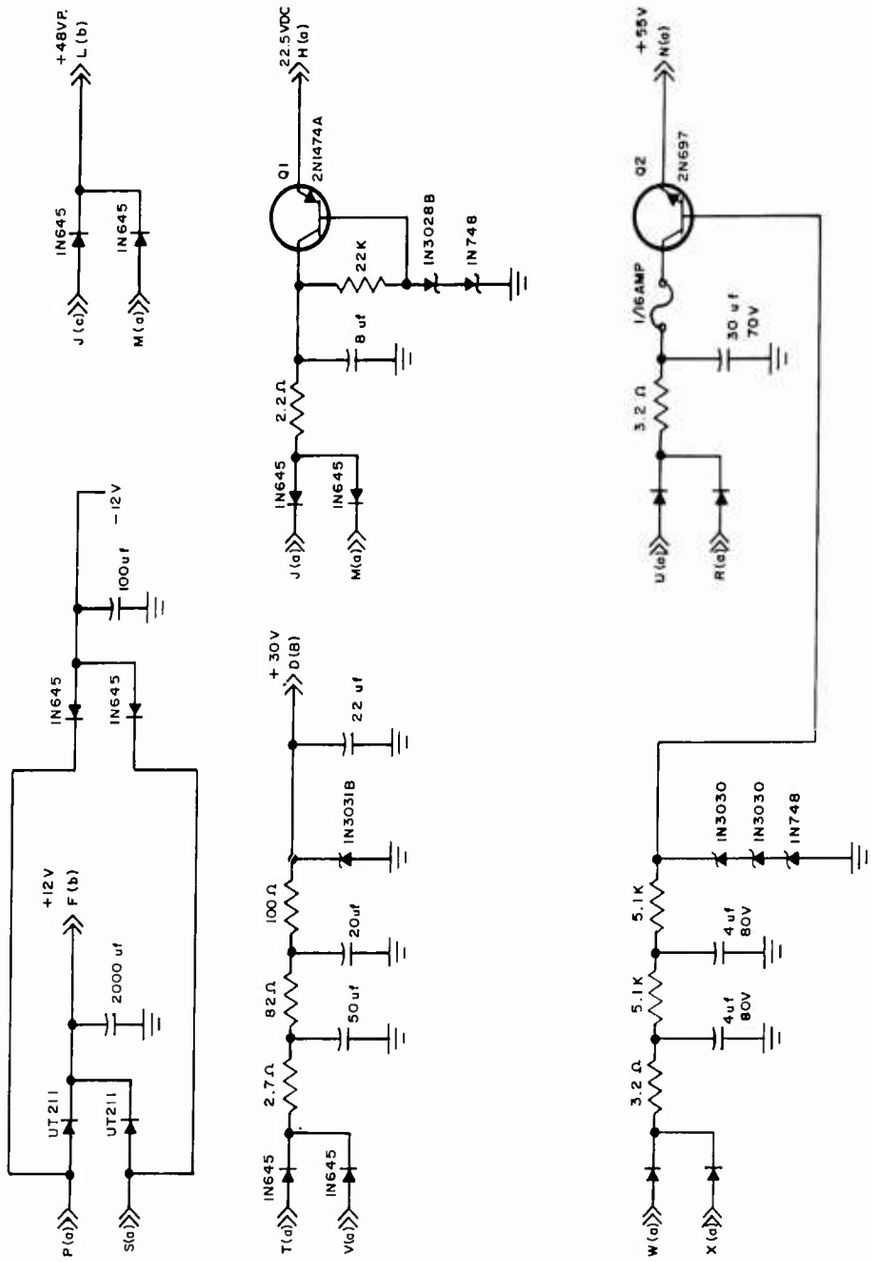
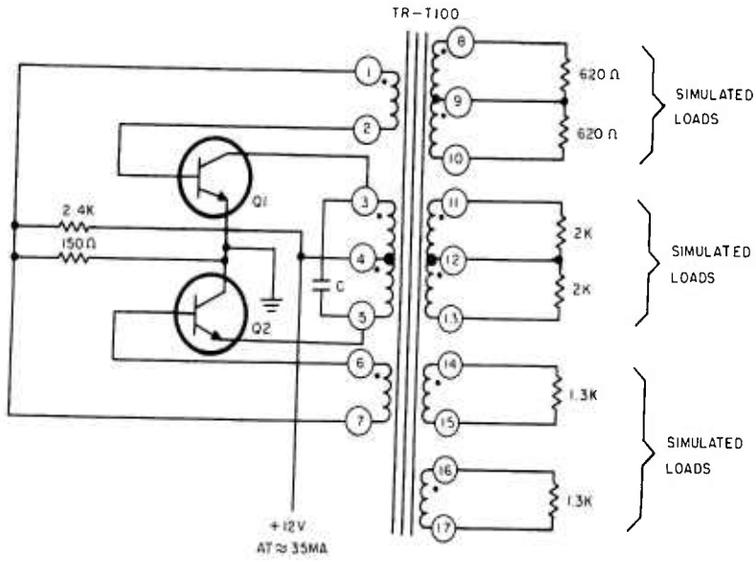


FIGURE 5-60. A-23 TRANSPONDER RECTIFIERS AND REGULATORS (SHEET 1 OF 2)

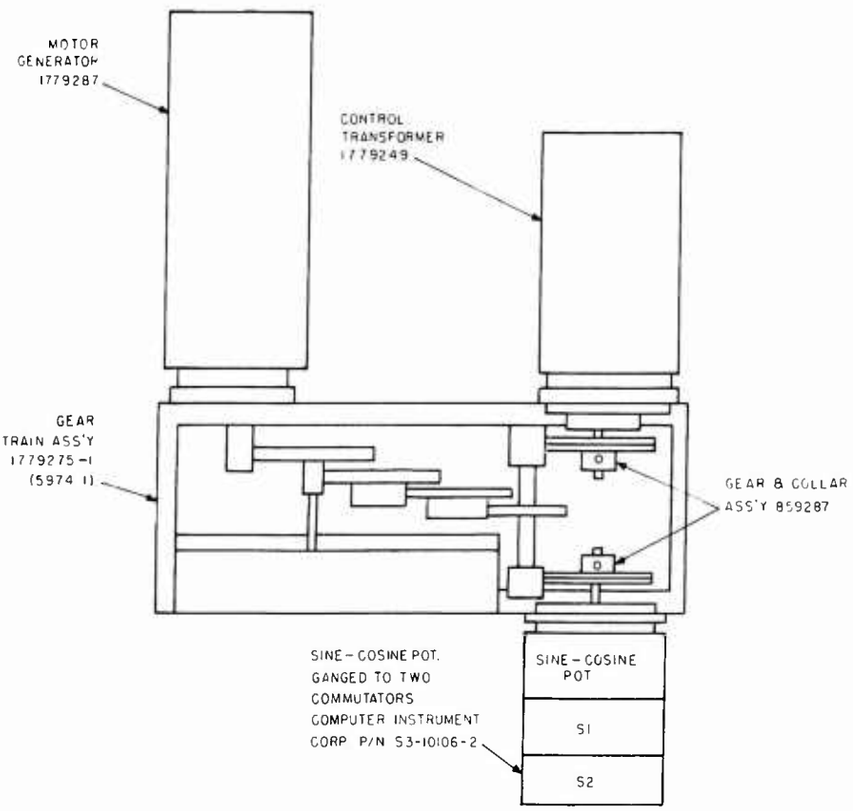


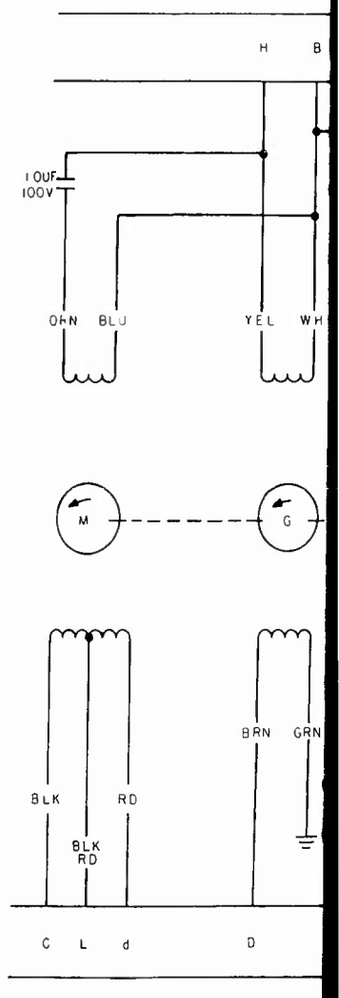
Q_1, Q_2 - - - - 2N2087

CAPACITOR "C" IS SELECTED AS REQUIRED

TO REDUCE SPIKES IF NECESSARY

FIGURE 5-60. A-23 TRANSPONDER RECTIFIERS AND REGULATORS (SHEET 2 OF 2)


MOTOR GENERATOR 1779287
CONTROL TRANSFORMER 1779249
GEAR TRAIN ASS'Y 1779275-1 (5974 1)
GEAR & COLLAR ASS'Y 859287
SINE-COSINE POT. GANGED TO TWO COMMUTATORS COMPUTER INSTRUMENT CORP P/N 53-10106-2
SINE-COSINE POT
S1
S2


H
B
1 OUF 100V
ORN
BLU
YEL
WH
M
G
BRN
GRN
BLK
RD
BLK RD
C
L
d
D


1

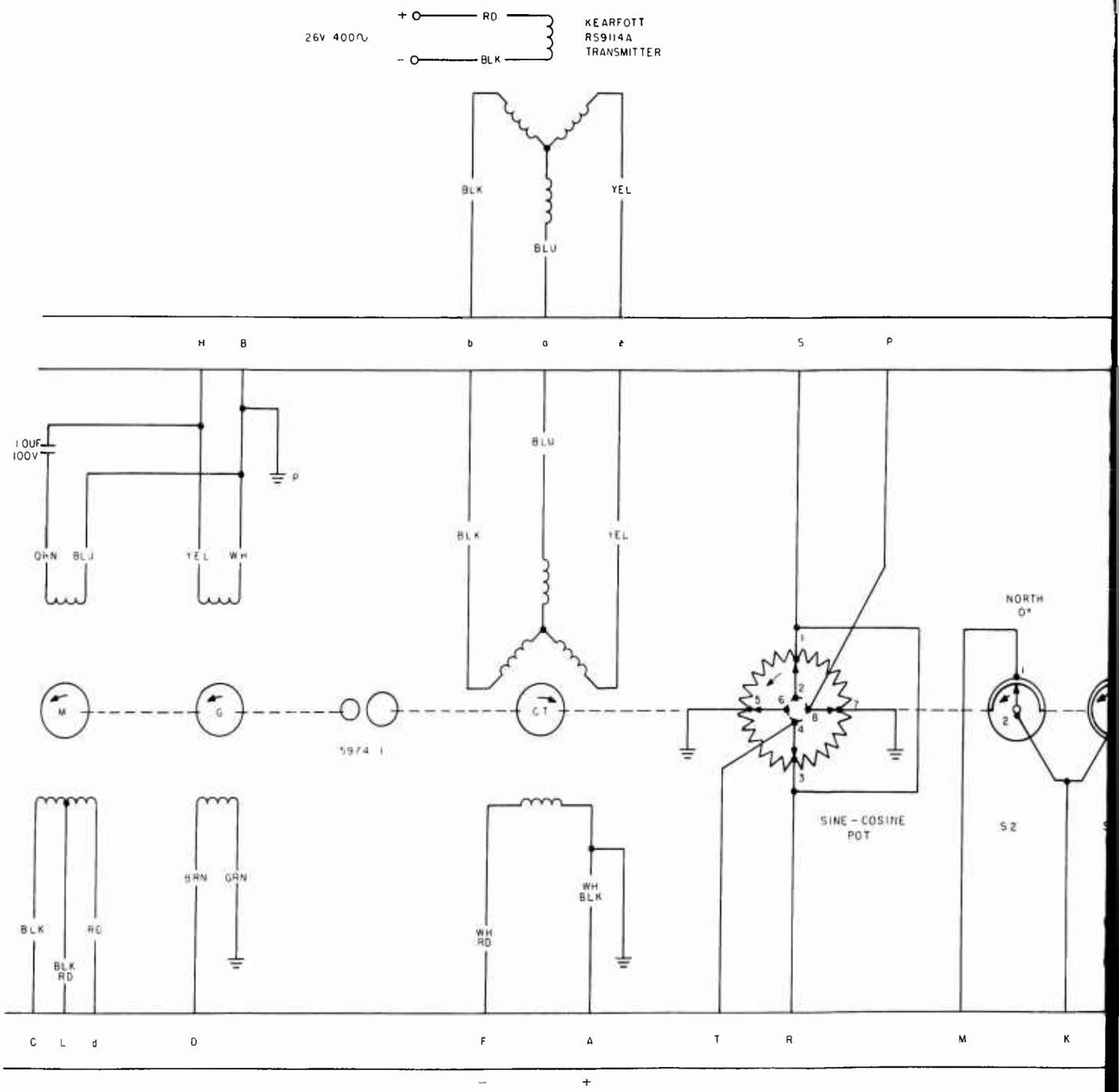


FIGURE 5-61

A-24 HEADING SERVO (α) FOR CAS T

2

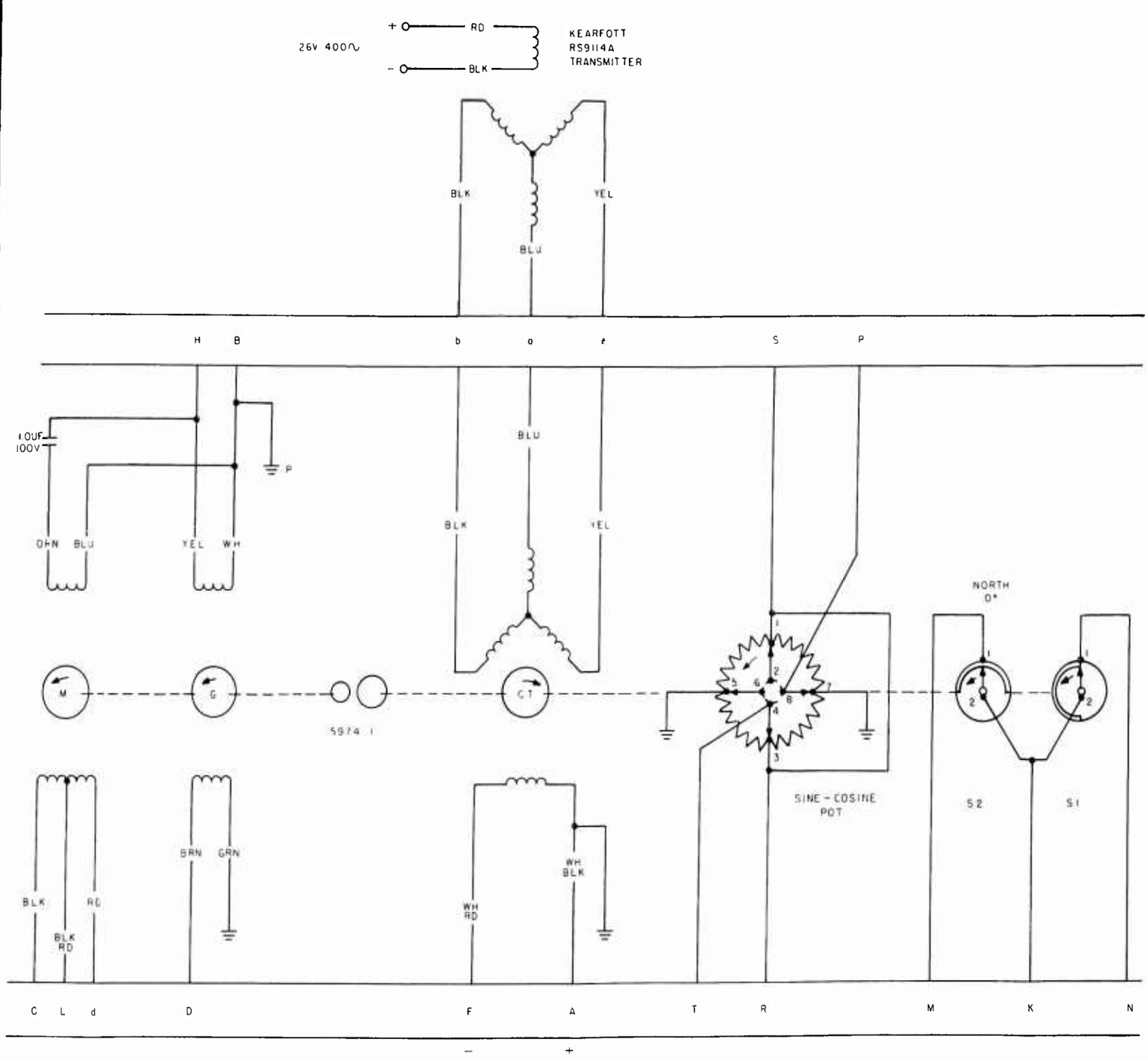


FIGURE 5-61

A-24 HEADING SERVO (α) FOR CAS TRANSPONDER

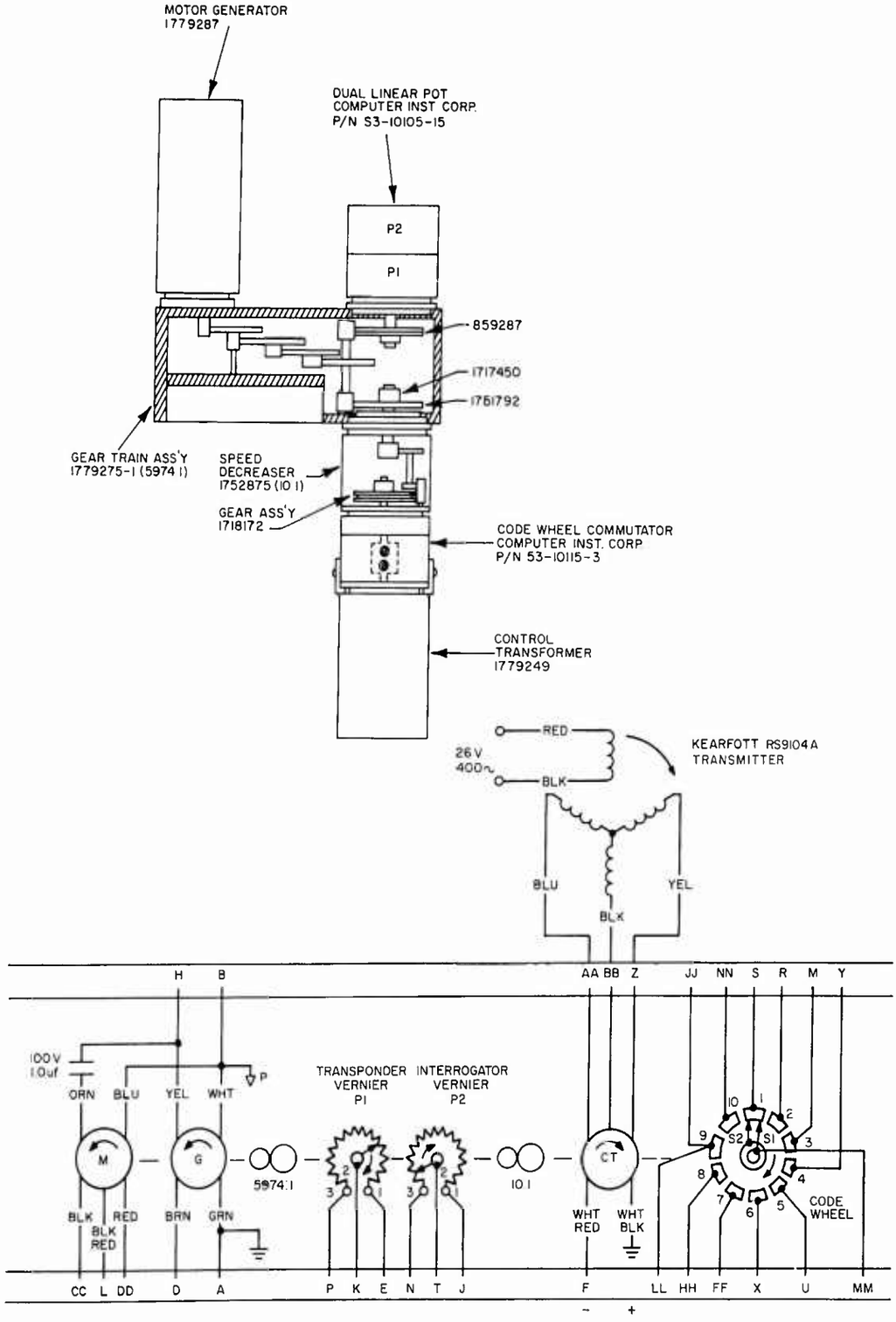
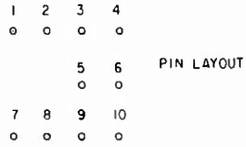
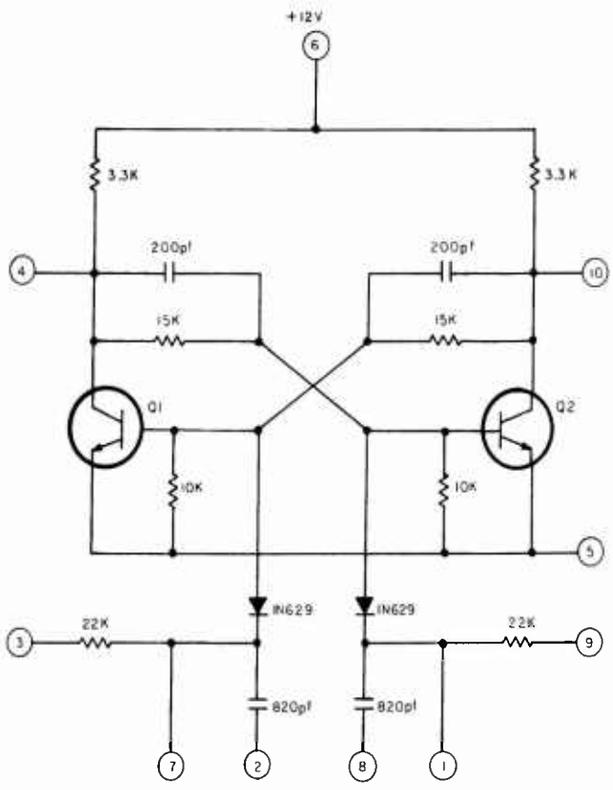


FIGURE 5-62 A-25 ALTITUDE SERVO (h) FOR CAS TRANSPONDER COMPUTER





Q_1, Q_2 — — — — 2N706

FIGURE 5-63. SATURATED FLIP-FLOP PN4282-6634

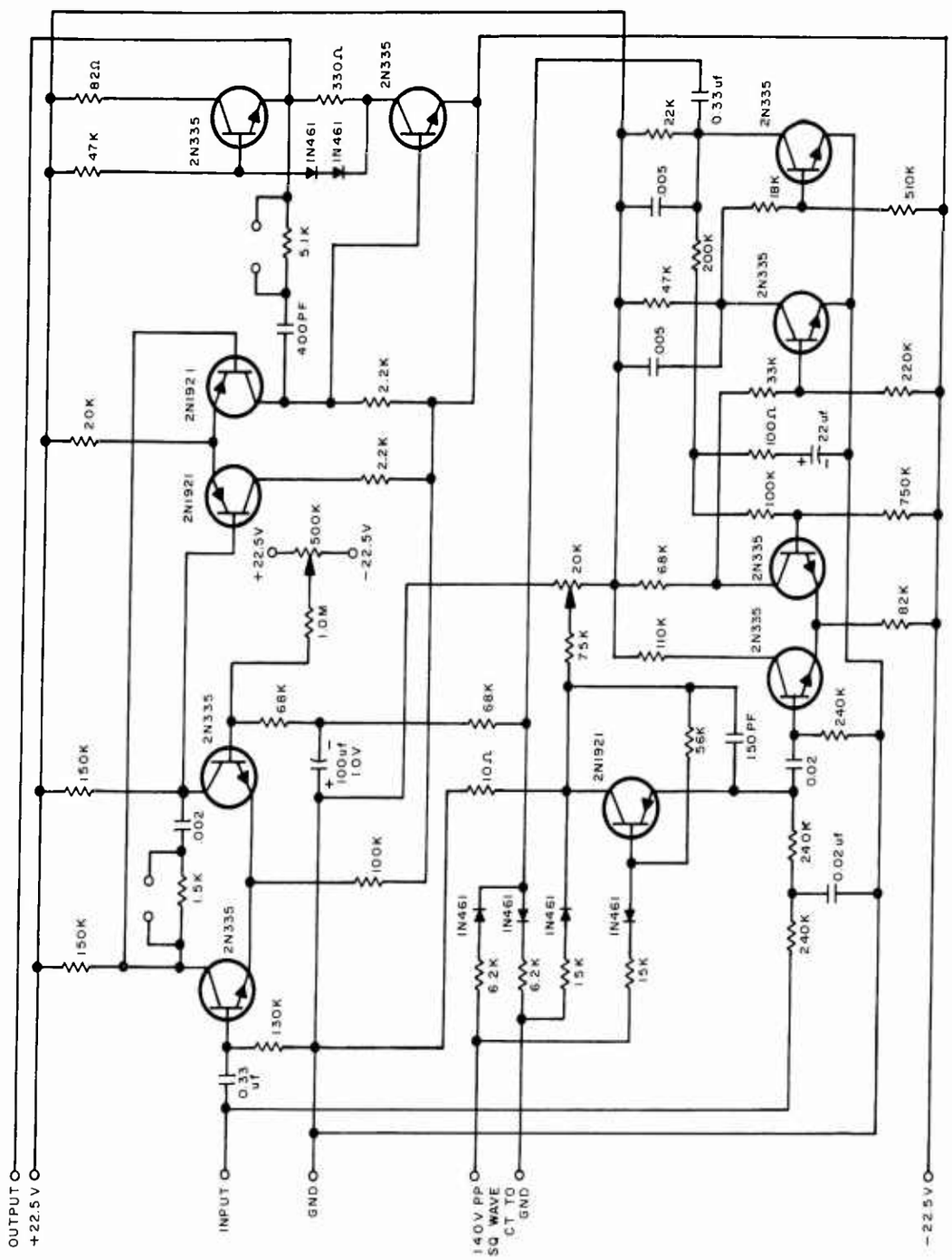


FIGURE 5-64. CHOPPER STABILIZED D-C OPERATIONAL AMPLIFIER

SECTION VI

OPERATION AND ALIGNMENT

A. OPERATION

Several items of special test equipment, or their equivalents, are necessary for operation of the breadboard equipment in a simulated encounter between two aircraft. These items of special test equipment and the functions they perform, are as follows:

- Test rack

  The test rack provides simulated electrical input data required by the system and simulates the effect of the scanning antenna. It also contains the overheard reply generator.

- Background noise generators and signal conditioners

  The background noise generators and signal conditioners provide random background noise signals to test their effect on the system, and generate properly shaped interrogation and reply pulses from the triggers generated by the breadboard encoders.

The following schematic information on these test units is included in this report:

- Test Rack Signal Schematic and System Interconnection Diagram Figure 6-1
- Test Rack Power Schematic Figure 6-2
- Interrogation Background Noise Generator and Signal Conditioner Figure 6-3
- Reply Background Noise Generator and Signal Conditioner Figure 6-4

In addition, schematics of electronic subassemblies of the test rack are included (figures 6-5 thru 6-7).

Some standard test equipment and power supplies are also required for operation, as detailed under Test Methods in Volume 1 of this report. Table 6-1

summarizes the power requirements of the breadboard coders and decoders. The breadboard computers have self-contained power supplies which operate from standard 115-volt, 400-cycle and 28-volt d-c sources.

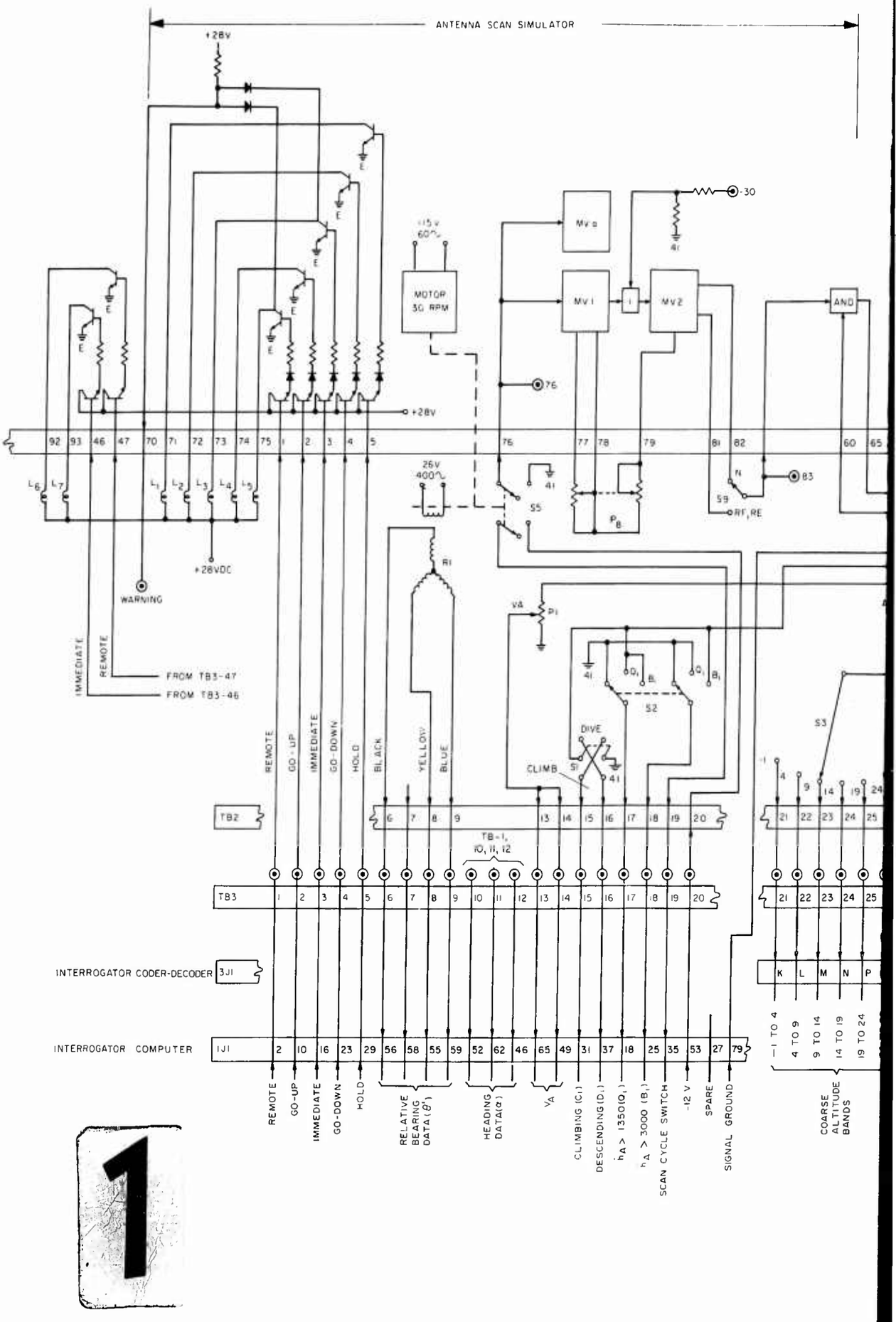
TABLE 6-1

CODER-DECODER POWER REQUIREMENTS

Supply Voltage	+30	-30	+12	-12
Interrogator (ma)	220	65	300	15
Transponder (ma)	200	20	300	10
Total (ma)	420	85	600	25

The primary controls used in operating the breadboard equipment are contained on the test rack. Figure 6-8 is a photograph of this rack with the various controls numbered. These controls are identified below by reference to these numbers, and operating instructions are included where necessary:

1. Interrogator Heading Reference Synchro
2., 3. Second Transponder Controls. Disconnected
4. Transponder Heading Reference Synchro
5. Variable Heading Drive Motor On-Off Switch. When variable heading is used, gears on transponder heading synchro (4) must be manually engaged using screw 4A.
6. Variable Altitude Drive Motor On-Off Switch
7. Interrogator Climb Rate Selector Switch
8. Antenna Scan Motor On-Off Switch
9. Interrogator Air Speed Control 0-300 Knots
10. Relative Bearing Reference Synchro
11. Interrogator Coarse Altitude Switch
12. Interrogator Vernier Altitude Control 0-5000 ft
13. Transponder Warning Lights
14. Interrogator Warning Lights
15. Transponder Vernier Altitude 0-5000 ft


ANTENNA SCAN SIMULATOR
+28V
MOTOR 30 RPM
MV0
MV1
MV2
AND
+28V
+28VDC
WARNING
IMMEDIATE
REMOTE
FROM TB3-47
FROM TB3-46
DIVE
CLIMB
BLACK
YELLOW
BLUE
TB2
TB3
INTERROGATOR CODER-DECODER 3J1
INTERROGATOR COMPUTER 1J1
REMOTE
GO-UP
IMMEDIATE
GO-DOWN
HOLD
RELATIVE BEARING DATA (β')
HEADING DATA (α)
VA
CLIMBING (C)
DESCENDING (D)
hA > 13501 (Q1)
hA > 3000 (B1)
SCAN CYCLE SWITCH
-12 V
SPARE
SIGNAL GROUND
COARSE ALTITUDE BANDS
1 TO 4
4 TO 9
9 TO 14
14 TO 19
19 TO 24

2

MV a

MV 1

1

MV 2

AND

-30

41

77 78 79 81 82 60 65 TB2

N

83

S9

RF, RE

P_8

⊙ TEST POINTS (FRONT PANEL)

RF - REPLY FAULTS
RE - REPLY ERRORS
} FALSE ALARM TESTS

N - NORMAL (COLLISION COMPUTATION AND MISS TESTS)

+30V

ALT VERNIER

P2

41

Q_1 B_1

S2

S3

DIVE

S1

+12V

-30V

101

TB1-94

TB1-97

TB1-3

14 15 16 17 18 19 20

21 22 23 24 25 26 27 28 29 30 31 52 TB3

K L M N P R S U E H D A F B C T X Z W V m k j h g f n b c d e p J3I

49 31 37 18 25 35 53 27 79

50 33 47 39 44 45 40 38 34 8 15 22 1 3 7 12 5 13 20 26 41 1J1

48 49 50 TB2

48 49 50 TB3

M T N J1403

APW-18 RANGE AND AZIMUTH INDICATOR

J1402 J1401

-1 TO 4
4 TO 9
9 TO 14
14 TO 19
19 TO 24
24 TO 29
29 TO 34
COARSE ALTITUDE BANDS

ALTITUDE VERNIER

+12 VDC

BAND COM

-30 VDC

SIGNAL AND POWER GROUND

-12 VDC

CHASSIS GROUND

+30 VDC REFERENCE

SPARE

MANEUVER RELAY

SPARE

$-V_{EB}$

SPARE

V_{EB}

$-V_{NB}$

V_{NB}

Q_t

U

L

SAMPLING GATE

REPLY PULSE NO 3

REPLY PULSE NO 7

RANGE DATA

VELOCITY POLARITY N

VELOCITY POLARITY S

VELOCITY POLARITY E

VELOCITY POLARITY W

BLANKING GATE

CLIMBING (C_1)

DESCENDING (D_1)

$h_A > 1350 (Q_1)$

$h_A > 3000 (B_1)$

SCAN CYCLE SWITCH

-12 V

SPARE

SIGNAL GROUND

MANEUVER RELAY

E VELOCITY (NEG)

E VELOCITY (POS)

N VELOCITY (NEG)

N VELOCITY (POS)

CHANGING -12

BELOW -10

ABOVE -8

SAMPLING GATE

REPLY TRIGGER

REPLY PULSE NO 7

RANGE VOLTAGE

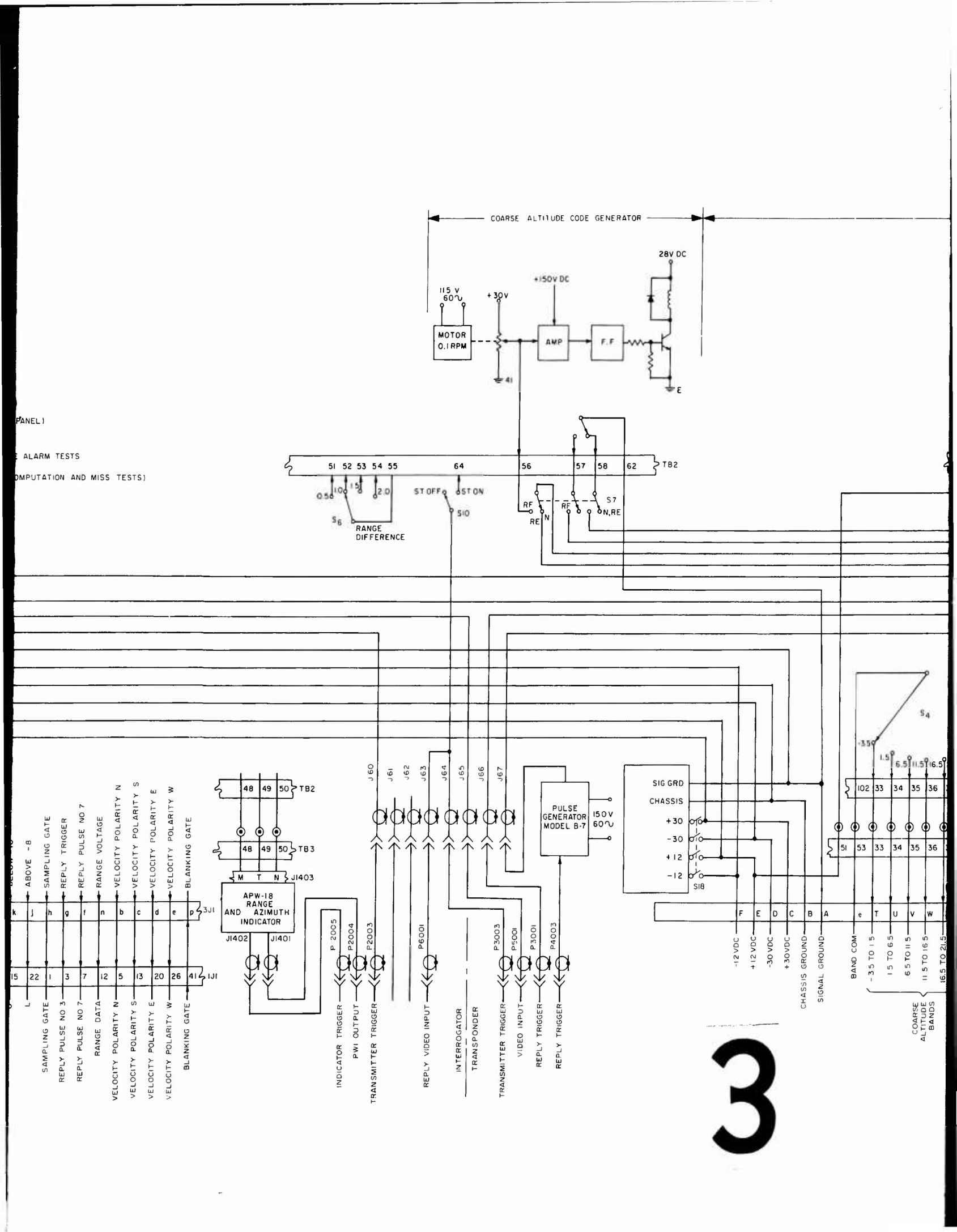
VELOCITY POLARITY N

VELOCITY POLARITY S

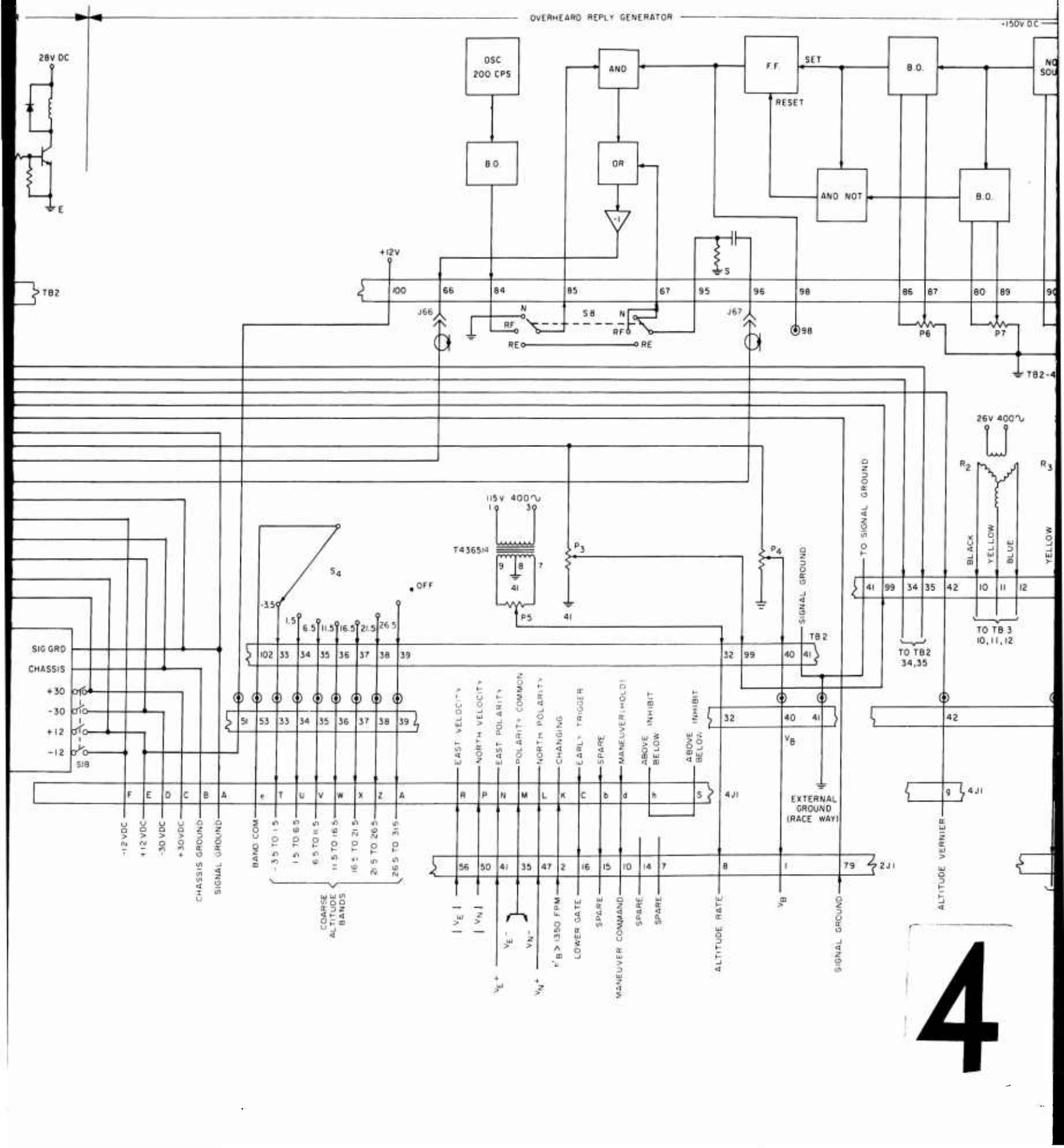
VELOCITY POLARITY E

VELOCITY POLARITY W

BLANKING GATE


COARSE ALTITUDE CODE GENERATOR
28V DC
115 V 60~
+30V
+150V DC
MOTOR 0.1 RPM
AMP
F.F
41
E
PANEL)
ALARM TESTS
OMPUTATION AND MISS TESTS)
51 52 53 54 55 64 56 57 58 62 TB2
0.5 1.0 1.5 2.0
ST OFF ST ON
S6
RANGE DIFFERENCE
S10
RF RE
RF
S7
N,RE
S4
-3.5
1.5 6.5 11.5 16.5
102 33 34 35 36
51 53 33 34 35 36
SIG GRD
CHASSIS
+30
-30
+12
-12
S18
PULSE GENERATOR MODEL B-7
150 V 60~
48 49 50 TB2
48 49 50 TB3
M T N J1403
APW-18 RANGE AND AZIMUTH INDICATOR
J1402 J1401
J60 J61 J62 J63 J64 J65 J66 J67
P 2005 P2004 P2003
P6001
P3003 P5001 P3001 P4003
k j h g f n b c d e p 3J1
15 22 1 3 7 12 5 13 20 26 41 1J1
ABOVE -8
SAMPLING GATE
REPLY TRIGGER
REPLY PULSE NO 7
RANGE VOLTAGE
VELOCITY POLARITY N
VELOCITY POLARITY S
VELOCITY POLARITY E
VELOCITY POLARITY W
BLANKING GATE
L
SAMPLING GATE
REPLY PULSE NO 3
REPLY PULSE NO 7
RANGE DATA
VELOCITY POLARITY N
VELOCITY POLARITY S
VELOCITY POLARITY E
VELOCITY POLARITY W
BLANKING GATE
INDICATOR TRIGGER
PWI OUTPUT
TRANSMITTER TRIGGER
REPLY VIDEO INPUT
INTERROGATOR
TRANSPONDER
TRANSMITTER TRIGGER
VIDEO INPUT
REPLY TRIGGER
REPLY TRIGGER
F E D C B A e T U V W
-12 VDC
+12 VDC
-30 VDC
+30VDC
CHASSIS GROUND
SIGNAL GROUND
BAND COM
-3.5 TO 1.5
1.5 TO 6.5
6.5 TO 11.5
11.5 TO 16.5
16.5 TO 21.5
COARSE ALTITUDE BANDS

3


OVERHEARD REPLY GENERATOR
+150V DC
28V DC
OSC 200 CPS
AND
F.F.
SET
RESET
B.O.
B.O
OR
AND NOT
B.O.
+12V
TB2
J66
J67
RF
RE
S8
P6
P7
TB2-4
26V 400~
115V 400~
T4365M
P3
P4
P5
S4
OFF
TO SIGNAL GROUND
SIGNAL GROUND
BLACK
YELLOW
BLUE
YELLOW
TO TB2 34,35
TO TB 3 10, 11, 12
SIG GRD
CHASSIS
+30
-30
+12
-12
S18
-12 VDC
+12 VDC
-30 VDC
+30 VDC
CHASSIS GROUND
SIGNAL GROUND
BAND COM
-3.5 TO 1.5
1.5 TO 6.5
6.5 TO 11.5
11.5 TO 16.5
16.5 TO 21.5
21.5 TO 26.5
26.5 TO 31.5
COARSE ALTITUDE BANDS
EAST VELOCITY
NORTH VELOCITY
EAST POLARITY
POLARITY COMMON
NORTH POLARITY
CHANGING
EARLY TRIGGER
SPARE
MANEUVER HOLD
ABOVE INHIBIT
BELOW
ABOVE INHIBIT
BELOW
4J1
2J1
V_E
V_N
V_E^-
V_N^-
V_E^+
V_N^+
$V_B > 1350$ FPM
LOWER GATE
SPARE
MANEUVER COMMAND
SPARE
SPARE
ALTITUDE RATE
V_B
V_B
EXTERNAL GROUND (RACE WAY)
SIGNAL GROUND
ALTITUDE VERNIER

4

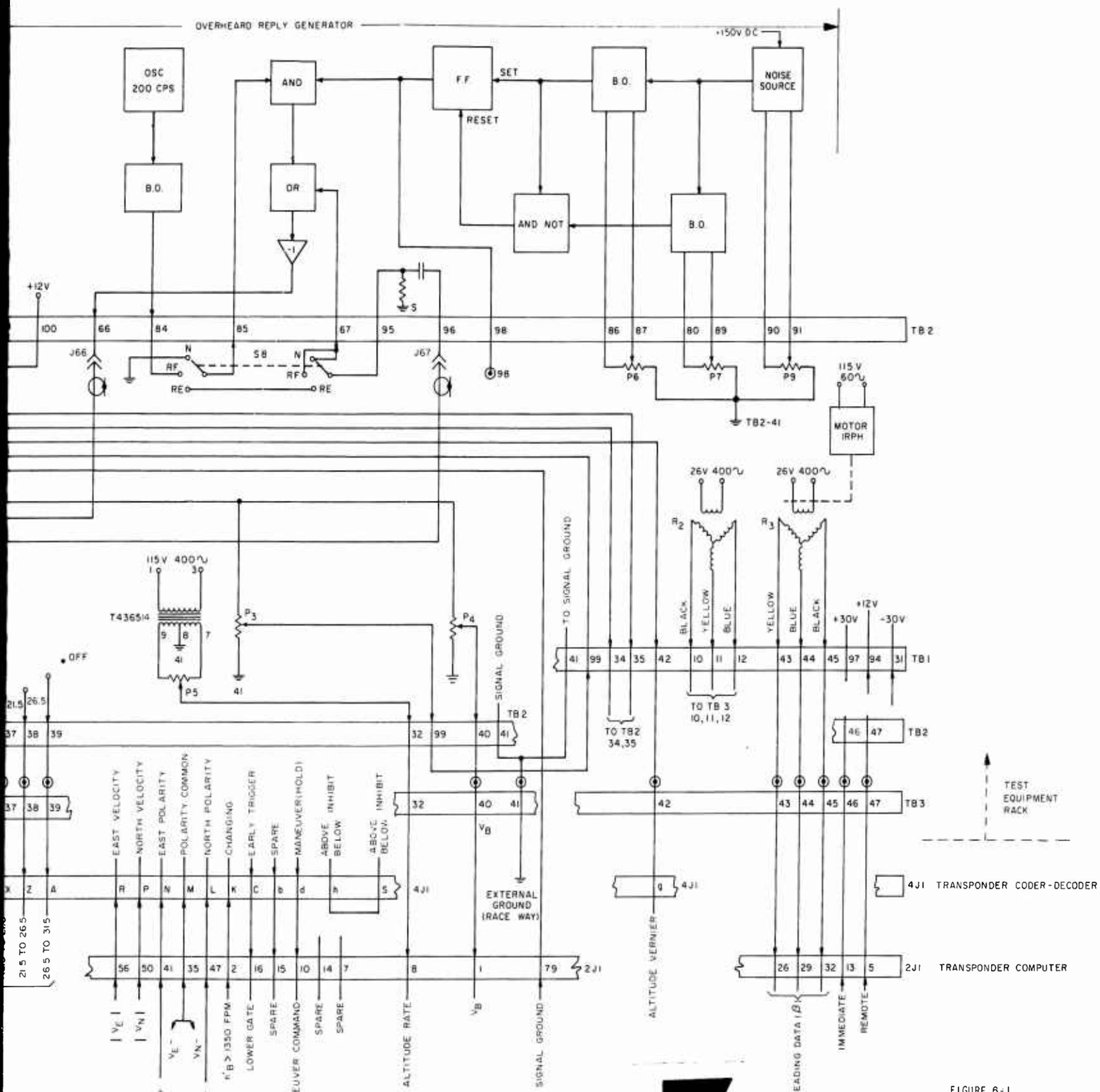
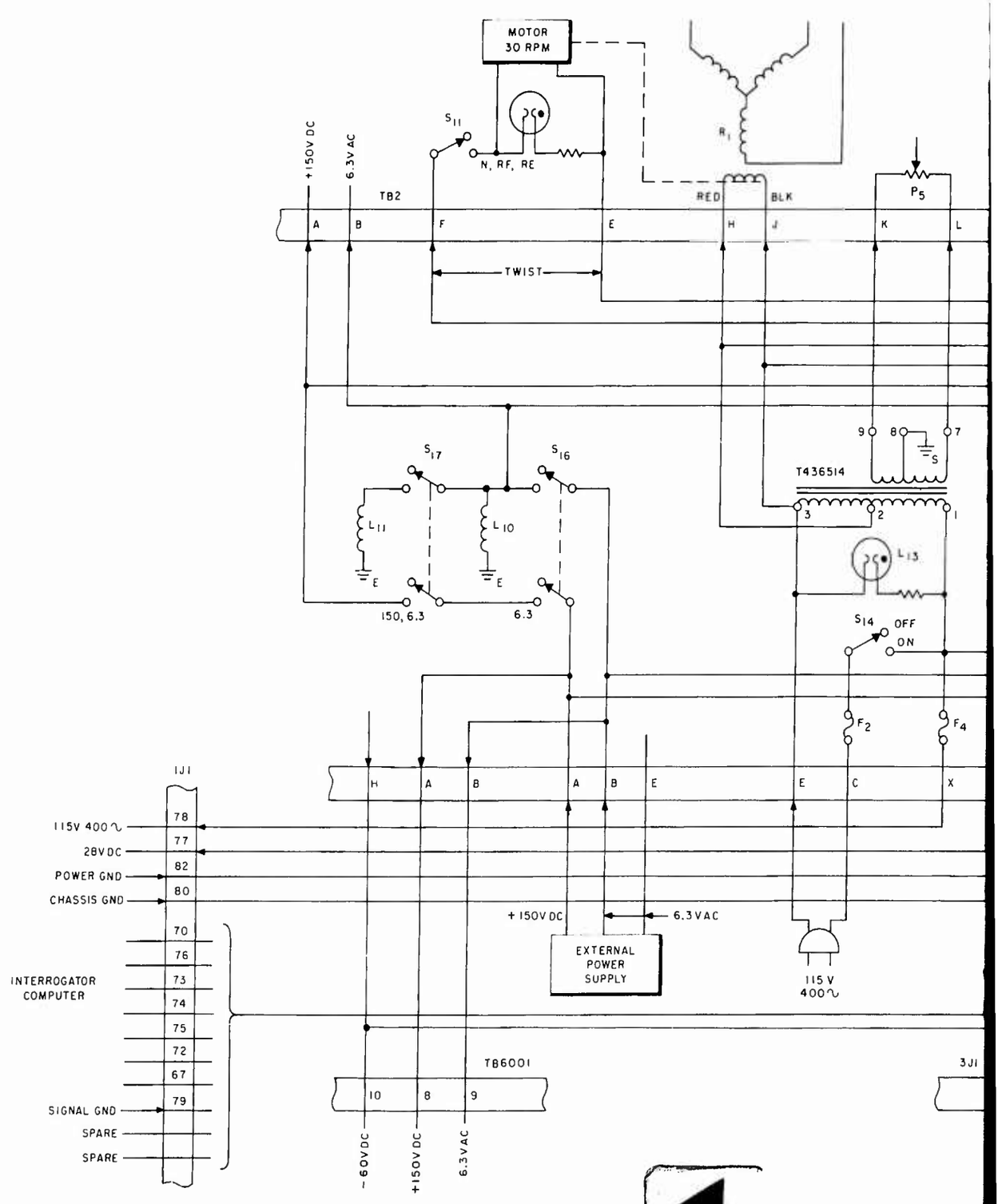
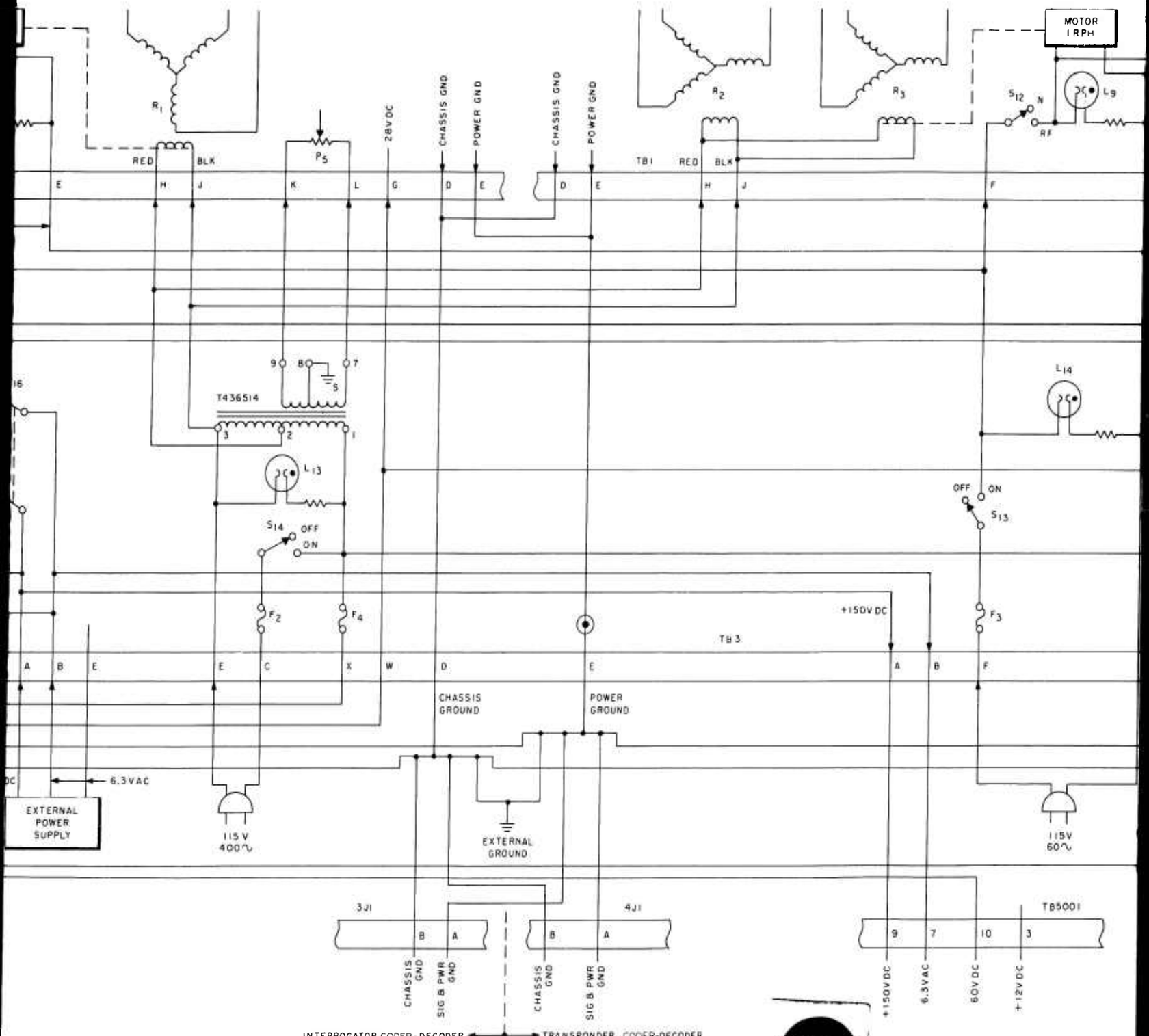


FIGURE 6-1

TEST RACK SIGNAL SCHEMATIC AND SYSTEM INTERCONNECTION DIAGRAM


MOTOR
30 RPM
S_{11}
N, RF, RE
R_1
+150V DC
6.3V AC
TB2
RED
BLK
P_5
A
B
F
E
H
J
K
L
TWIST
9
8
7
S
T436514
3
2
1
S_{17}
S_{16}
L_{11}
L_{10}
L_{13}
E
150, 6.3
6.3
S_{14}
OFF
ON
F_2
F_4
1J1
H
A
B
A
B
E
E
C
X
115V 400∿
28V DC
POWER GND
CHASSIS GND
78
77
82
80
70
76
73
74
75
72
67
79
INTERROGATOR
COMPUTER
SIGNAL GND
SPARE
SPARE
+150V DC
6.3VAC
EXTERNAL
POWER
SUPPLY
115 V
400∿
TB6001
10
8
9
3J1
-60V DC
+150V DC
6.3VAC


MOTOR
1 RPH
R1
R2
R3
P5
28V DC
CHASSIS GND
POWER GND
CHASSIS GND
POWER GND
TB1
RED
BLK
RED
BLK
S12
N
RF
L9
L14
T436514
9
8
7
S
3
2
1
L13
S14
OFF
ON
OFF
ON
S13
F2
F4
F3
+150V DC
TB3
A
B
E
E
C
X
W
D
E
A
B
F
CHASSIS
GROUND
POWER
GROUND
6.3VAC
EXTERNAL
POWER
SUPPLY
115 V
400~
EXTERNAL
GROUND
115V
60~
3J1
4J1
TB5001
B
A
B
A
9
7
10
3
CHASSIS GND
SIG B PWR GND
CHASSIS GND
SIG B PWR GND
+150V DC
6.3VAC
60V DC
+12V DC
INTERROGATOR CODER-DECODER
TRANSPONDER CODER-DECODER

2

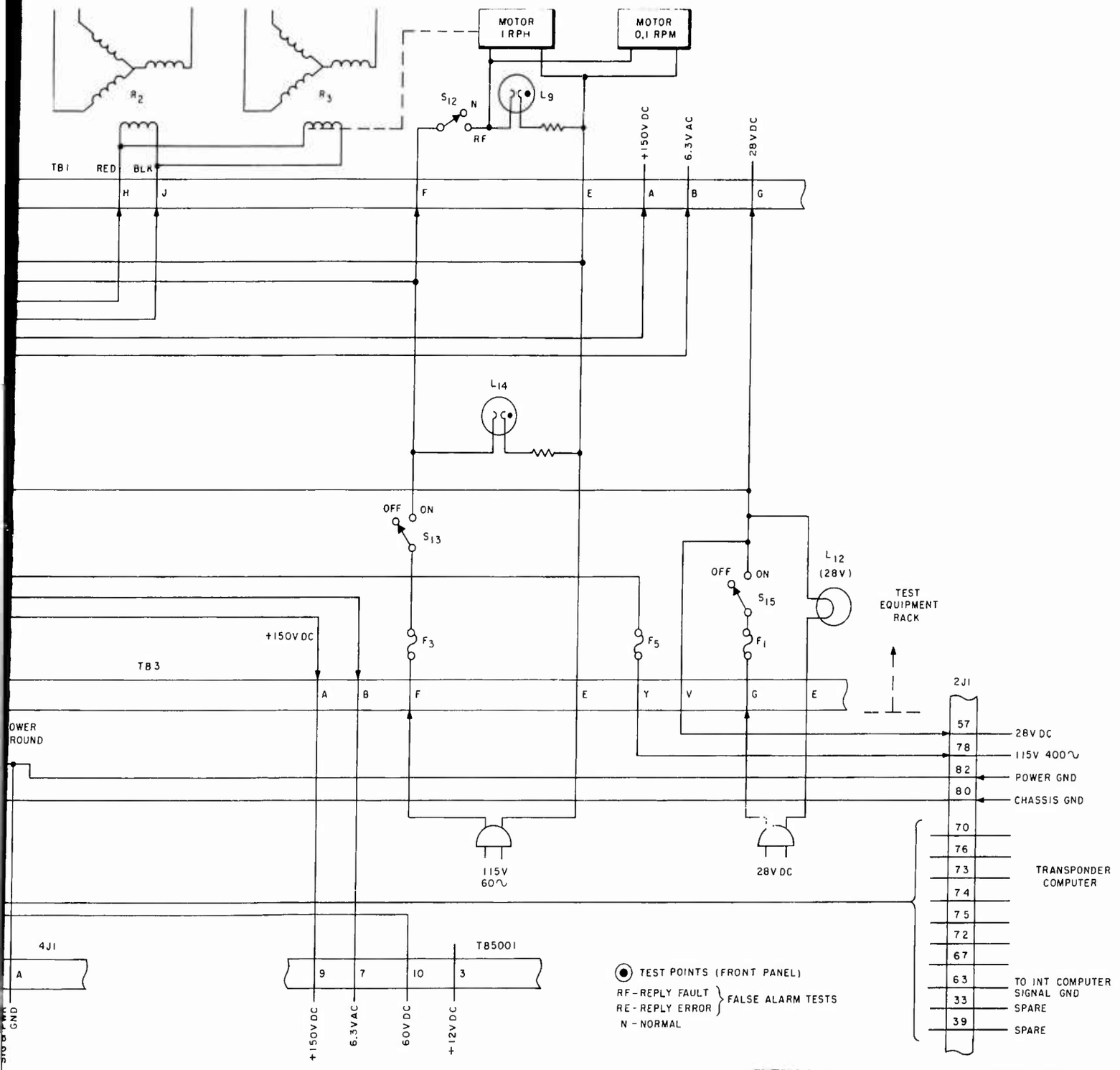
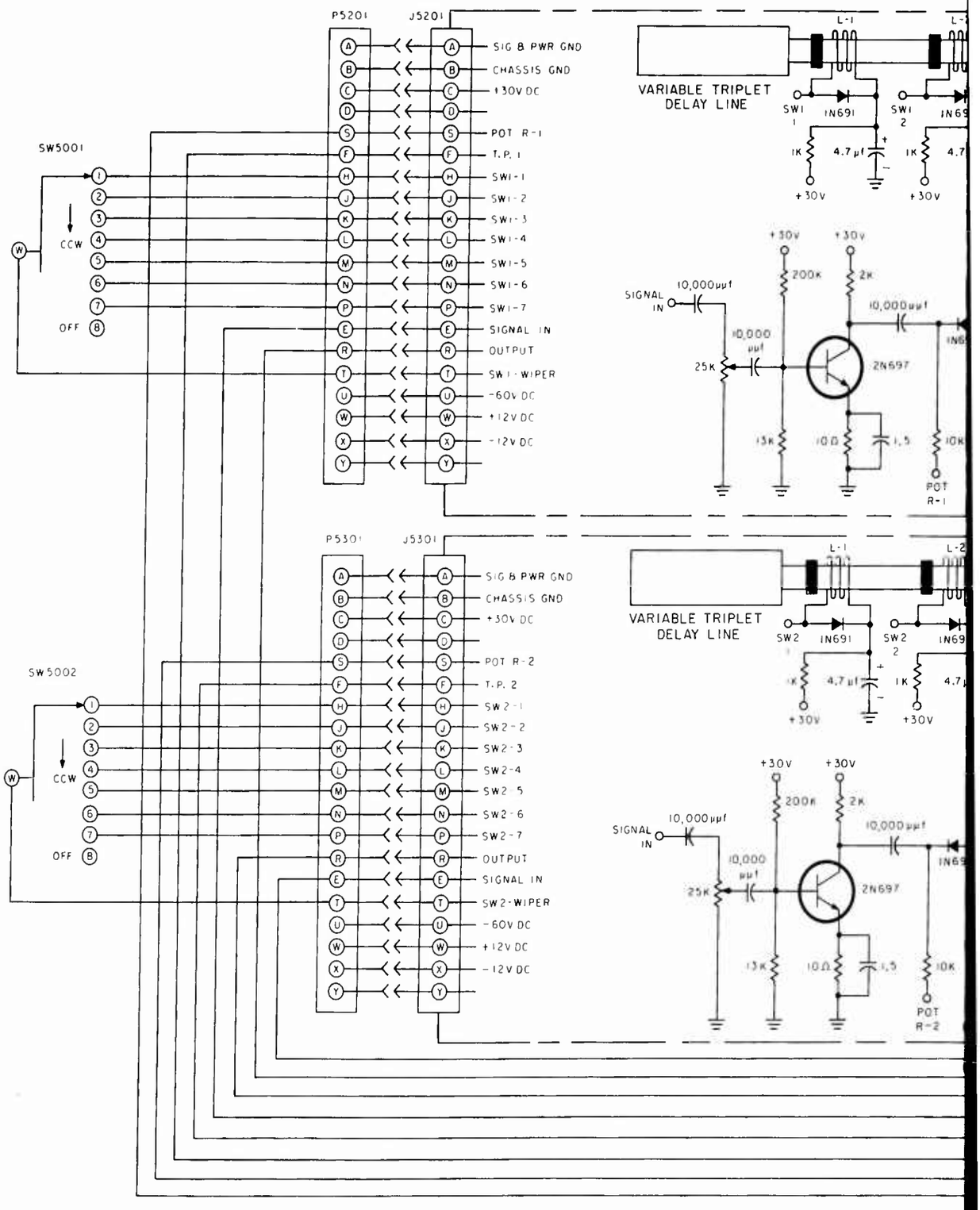
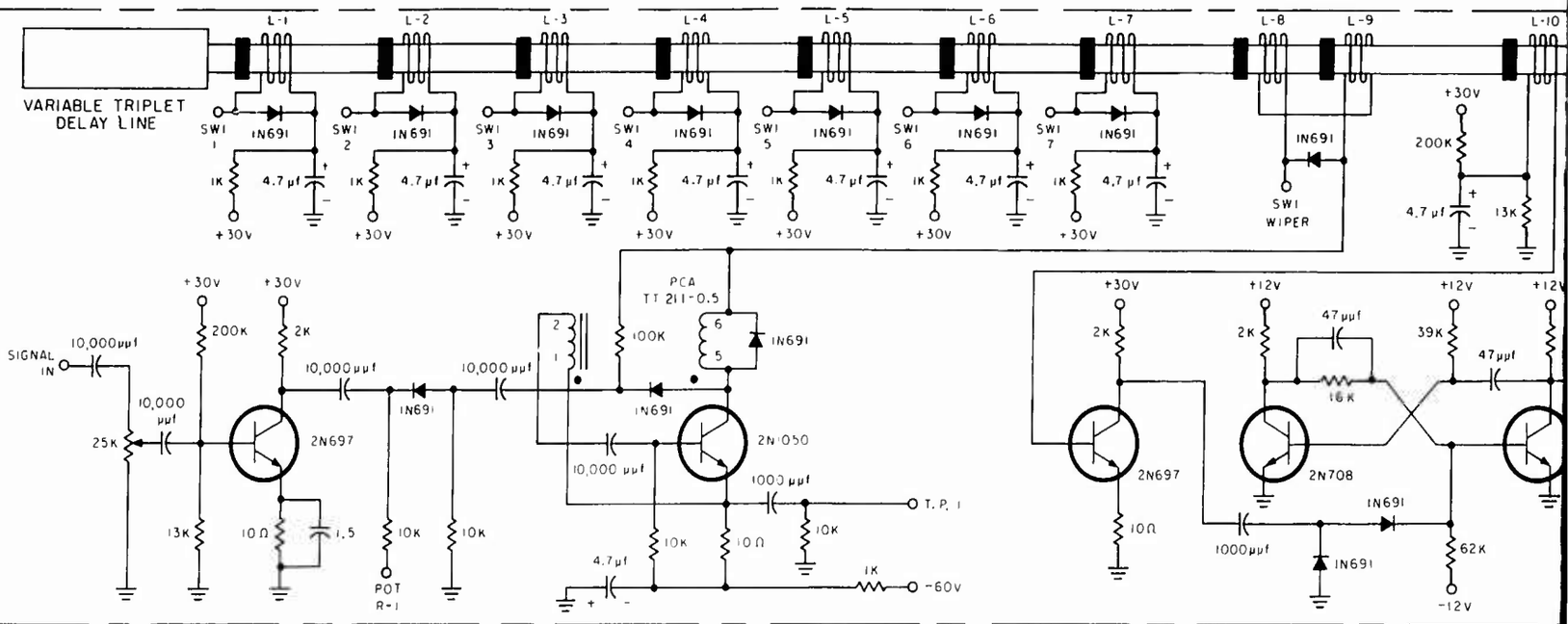


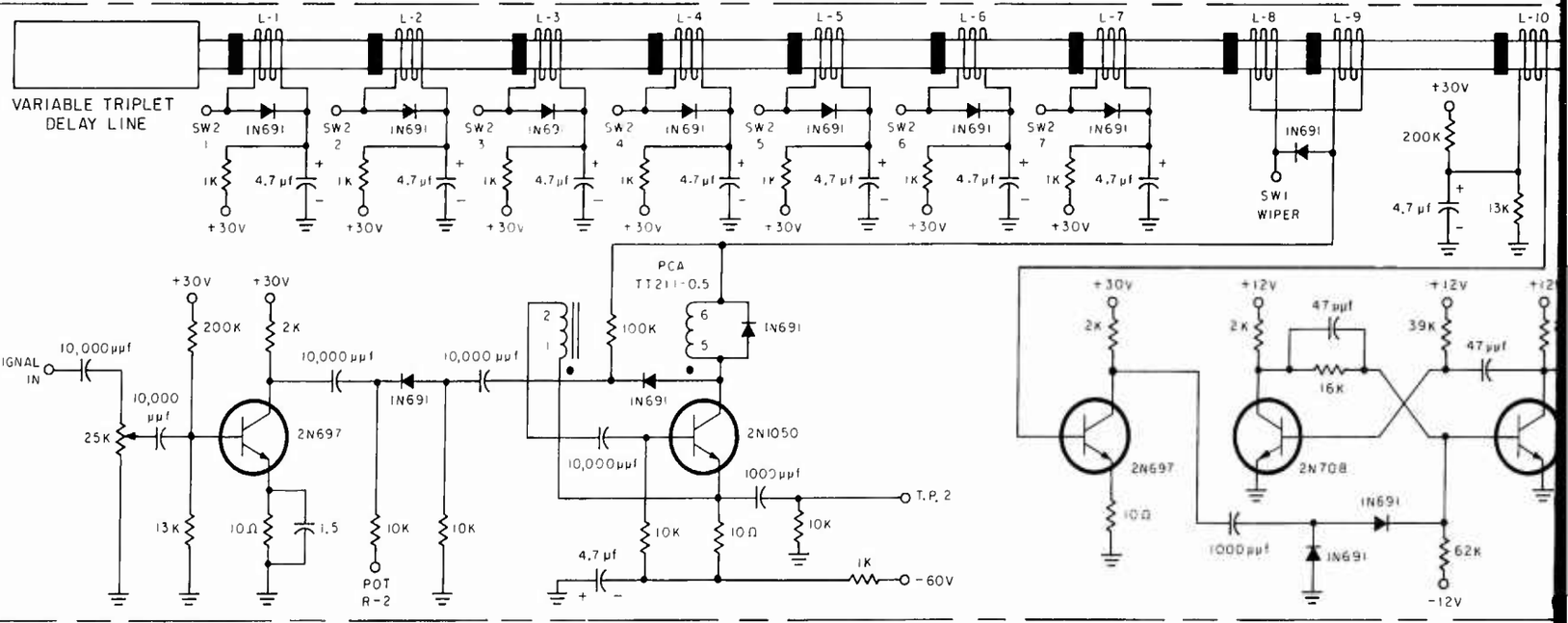
FIGURE 6-2

TEST RACK POWER SCHEMATIC


P5201
J5201
SIG B PWR GND
CHASSIS GND
+30V DC
POT R-1
T.P. 1
SW1-1
SW1-2
SW1-3
SW1-4
SW1-5
SW1-6
SW1-7
SIGNAL IN
OUTPUT
SW1-WIPER
-60V DC
+12V DC
-12V DC
SW5001
CCW
OFF
VARIABLE TRIPLET DELAY LINE
L-1
L-2
SW1
IN691
1K
4.7μf
+30V
SIGNAL IN
10,000μμf
200K
2K
25K
2N697
13K
100
1.5
10K
POT R-1
P5301
J5301
SIG B PWR GND
CHASSIS GND
+30V DC
POT R-2
T.P. 2
SW2-1
SW2-2
SW2-3
SW2-4
SW2-5
SW2-6
SW2-7
OUTPUT
SIGNAL IN
SW2-WIPER
-60V DC
+12V DC
-12V DC
SW5002
CCW
OFF
VARIABLE TRIPLET DELAY LINE
SW2
IN691
1K
4.7μf
+30V
SIGNAL IN
10,000μμf
200K
2K
25K
2N697
13K
100
1.5
10K
POT R-2

1





2

INTERROGATION B
SIGNAL CON

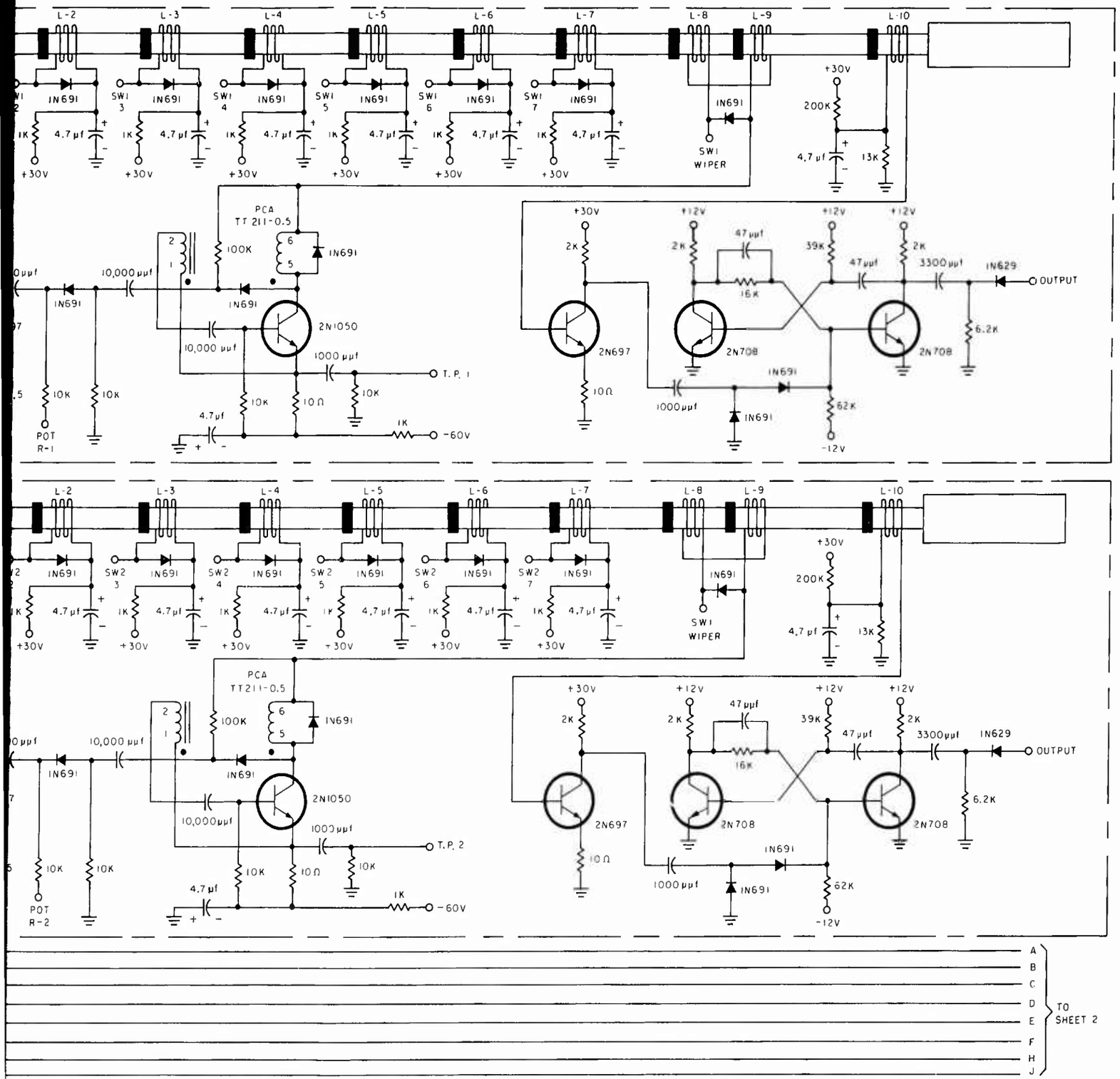
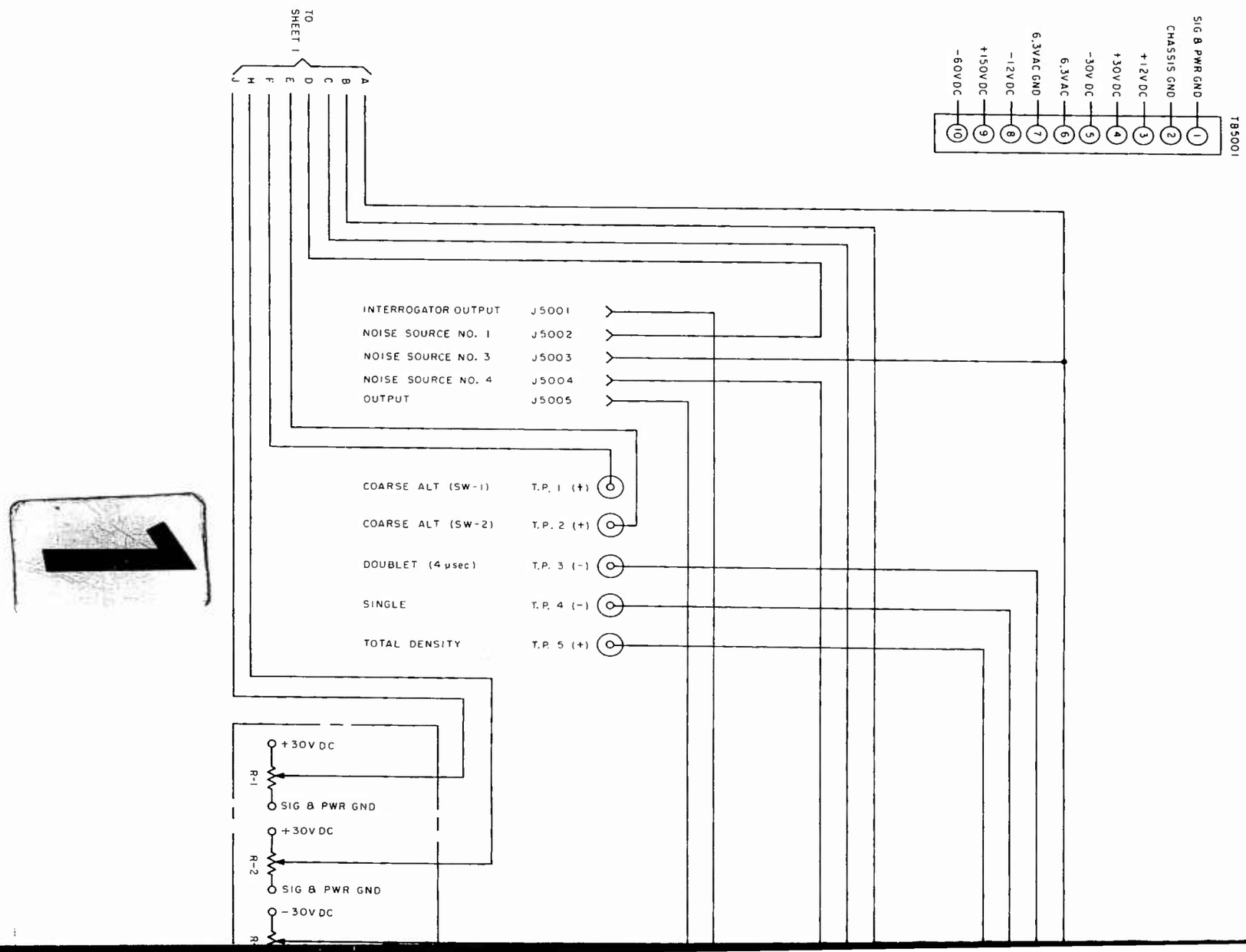
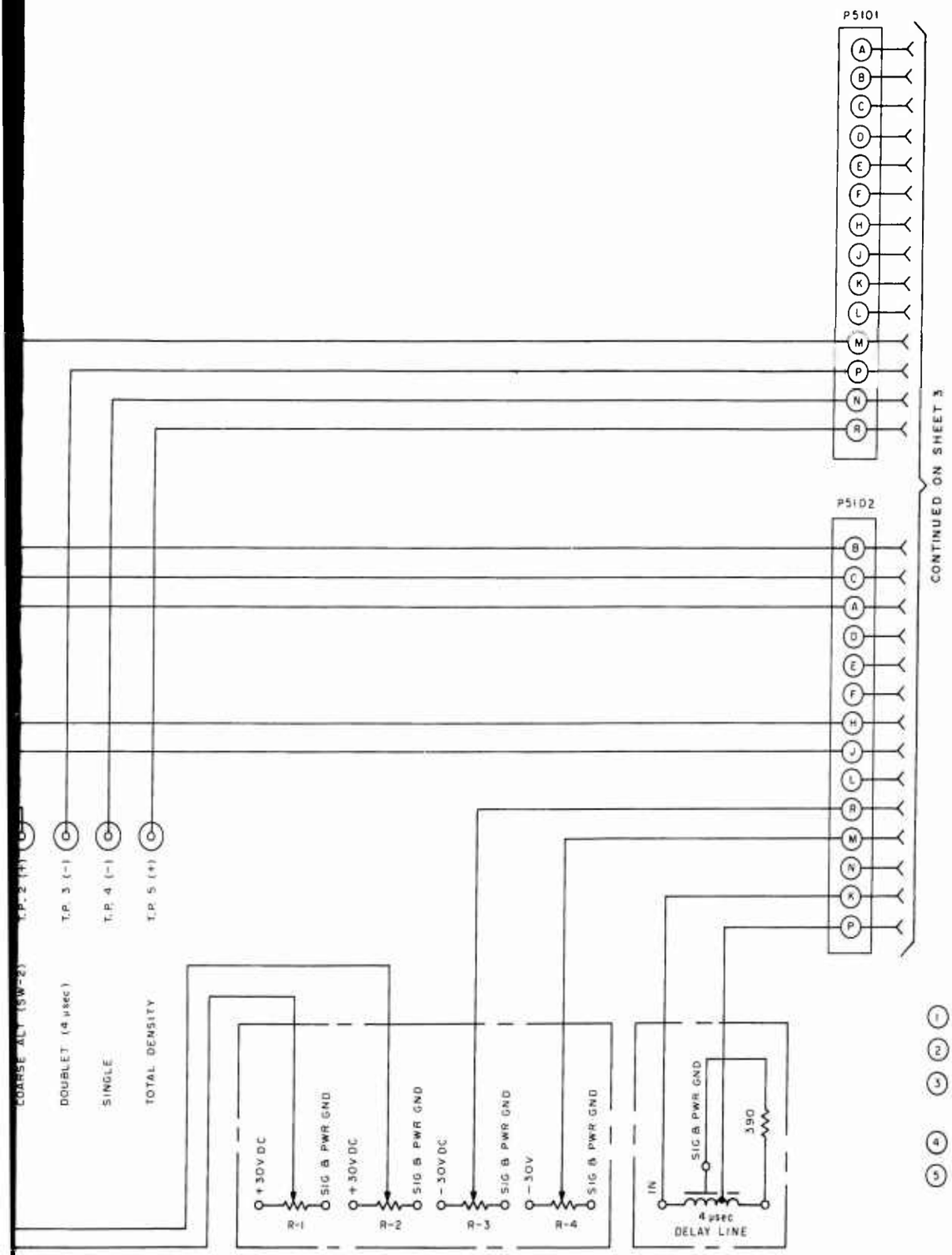


FIGURE 6-3

INTERROGATION BACKGROUND NOISE GENERATOR AND SIGNAL CONDITIONER (SHEET 1 OF 3)

3


TO SHEET 1
J H F E D C B A
SIG & PWR GND
CHASSIS GND
+12V DC
+30V DC
-30V DC
6.3VAC
6.3VAC GND
-12V DC
+150V DC
-60V DC
TB5001
INTERROGATOR OUTPUT J5001
NOISE SOURCE NO. 1 J5002
NOISE SOURCE NO. 3 J5003
NOISE SOURCE NO. 4 J5004
OUTPUT J5005
COARSE ALT (SW-1) T.P. 1 (+)
COARSE ALT (SW-2) T.P. 2 (+)
DOUBLET (4 μsec) T.P. 3 (-)
SINGLE T.P. 4 (-)
TOTAL DENSITY T.P. 5 (+)
+30V DC
R-1
SIG & PWR GND
+30V DC
R-2
SIG & PWR GND
-30V DC



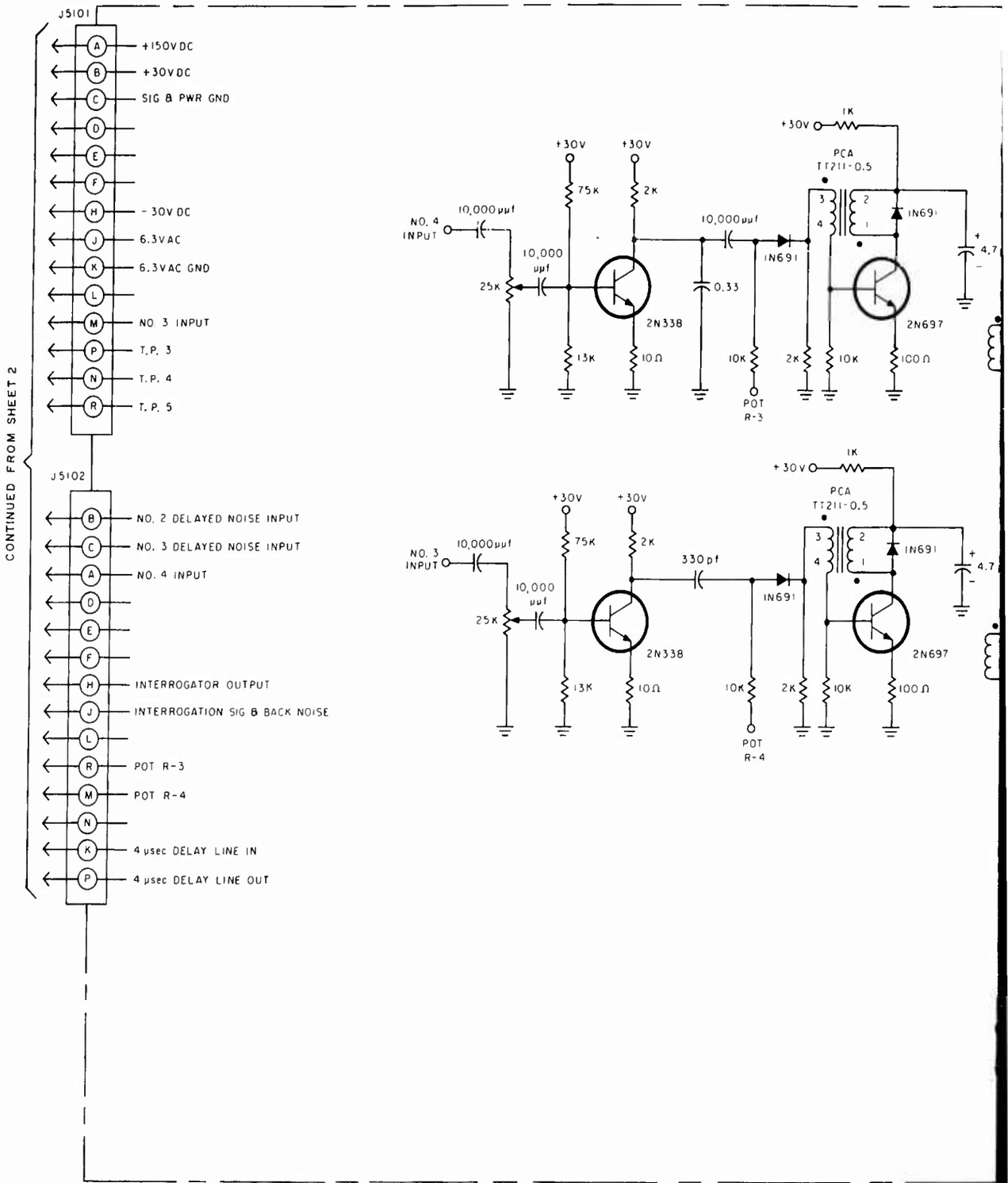
2

NOTES:

1. POWER INTERCONNECTIONS NOT SHOWN
2. R1-R4 100K 1W POTS
3. DELAY LINE ASSY NO'S: COIL MOUNT ASSY. 4240-00147
   PAD BASE 4240-00143
   PAD COVER 4240-00144
4. ALL TRANSFORMERS PCA ELECTRONICS TYPE AS SHOWN
5. DELAY LINES: 0.5 μsec PCA TYPE DL10000-0.5 RMT
   4 μsec DWG NO. 4240-00174

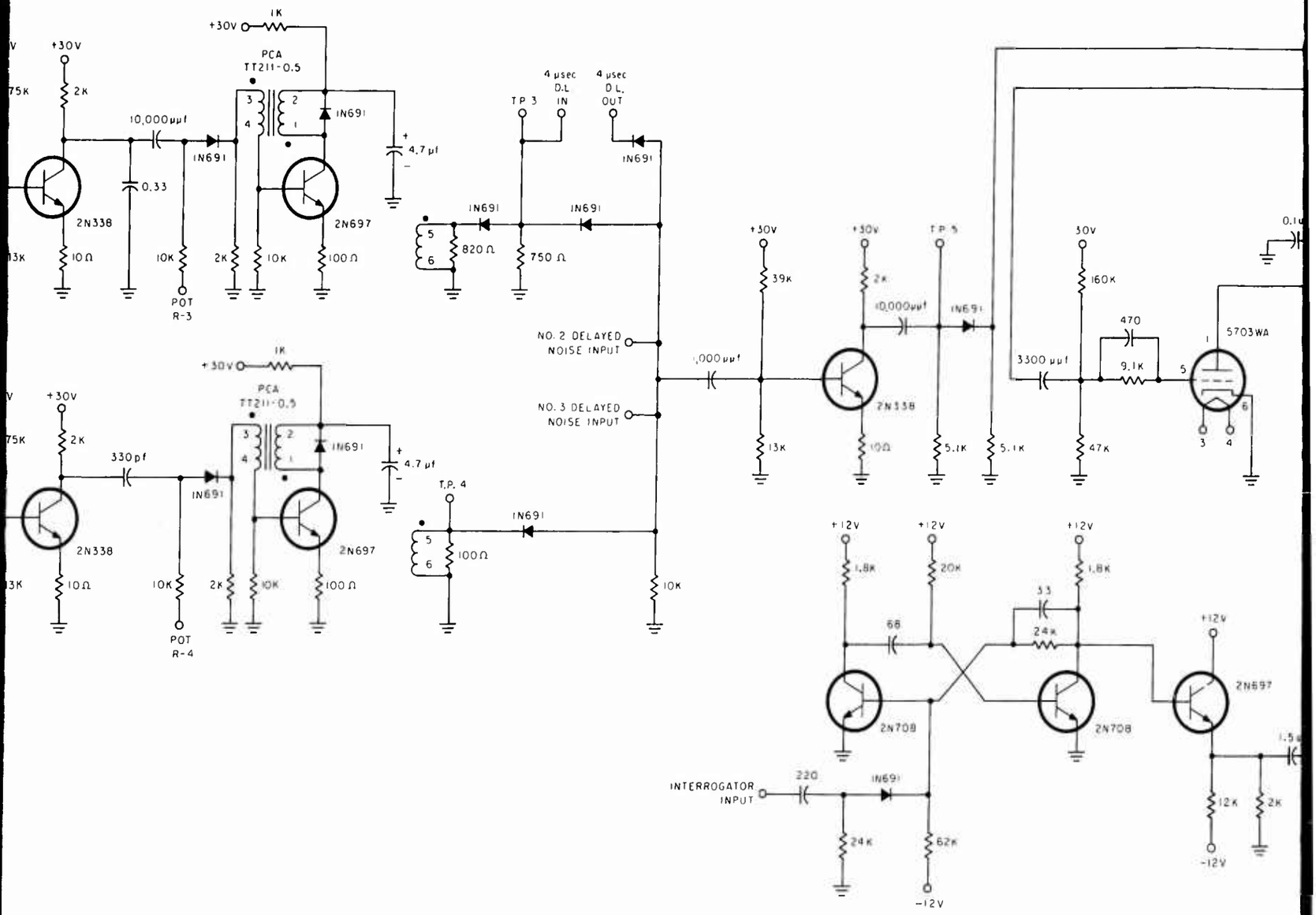
FIGURE 6-3

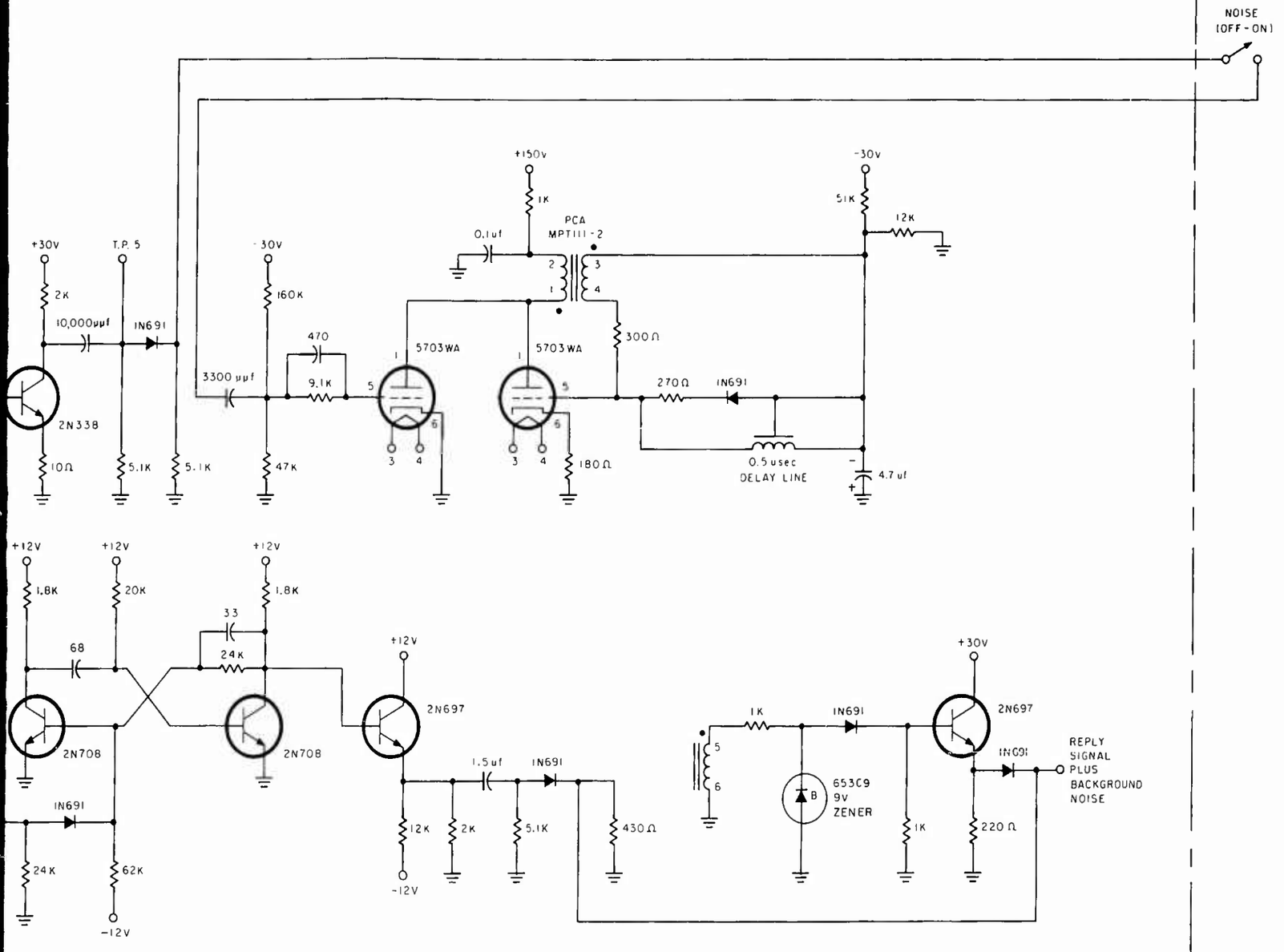
INTERROGATION BACKGROUND NOISE GENERATOR AND SIGNAL CONDITIONER (SHEET 2 OF 3)


J5101
A +150V DC
B +30V DC
C SIG & PWR GND
D
E
F
H - 30V DC
J 6.3VAC
K 6.3VAC GND
L
M NO. 3 INPUT
P T.P. 3
N T.P. 4
R T.P. 5
J5102
B NO. 2 DELAYED NOISE INPUT
C NO. 3 DELAYED NOISE INPUT
A NO. 4 INPUT
D
E
F
H INTERROGATOR OUTPUT
J INTERROGATION SIG & BACK NOISE
L
R POT R-3
M POT R-4
N
K 4 μsec DELAY LINE IN
P 4 μsec DELAY LINE OUT
CONTINUED FROM SHEET 2
NO. 4 INPUT
10,000 μμf
25K
10,000 μμf
+30V
75K
13K
2K
10Ω
2N338
10,000 μμf
0.33
IN691
10K
POT R-3
1K
+30V
PCA TT211-0.5
IN691
2K
10K
2N697
100Ω
4.7
NO. 3 INPUT
10,000 μμf
25K
10,000 μμf
+30V
75K
13K
2K
10Ω
2N338
330 pf
IN691
10K
POT R-4
1K
+30V
PCA TT211-0.5
IN691
2K
10K
2N697
100Ω
4.7

1

LOGIC CIRCUIT BOARD

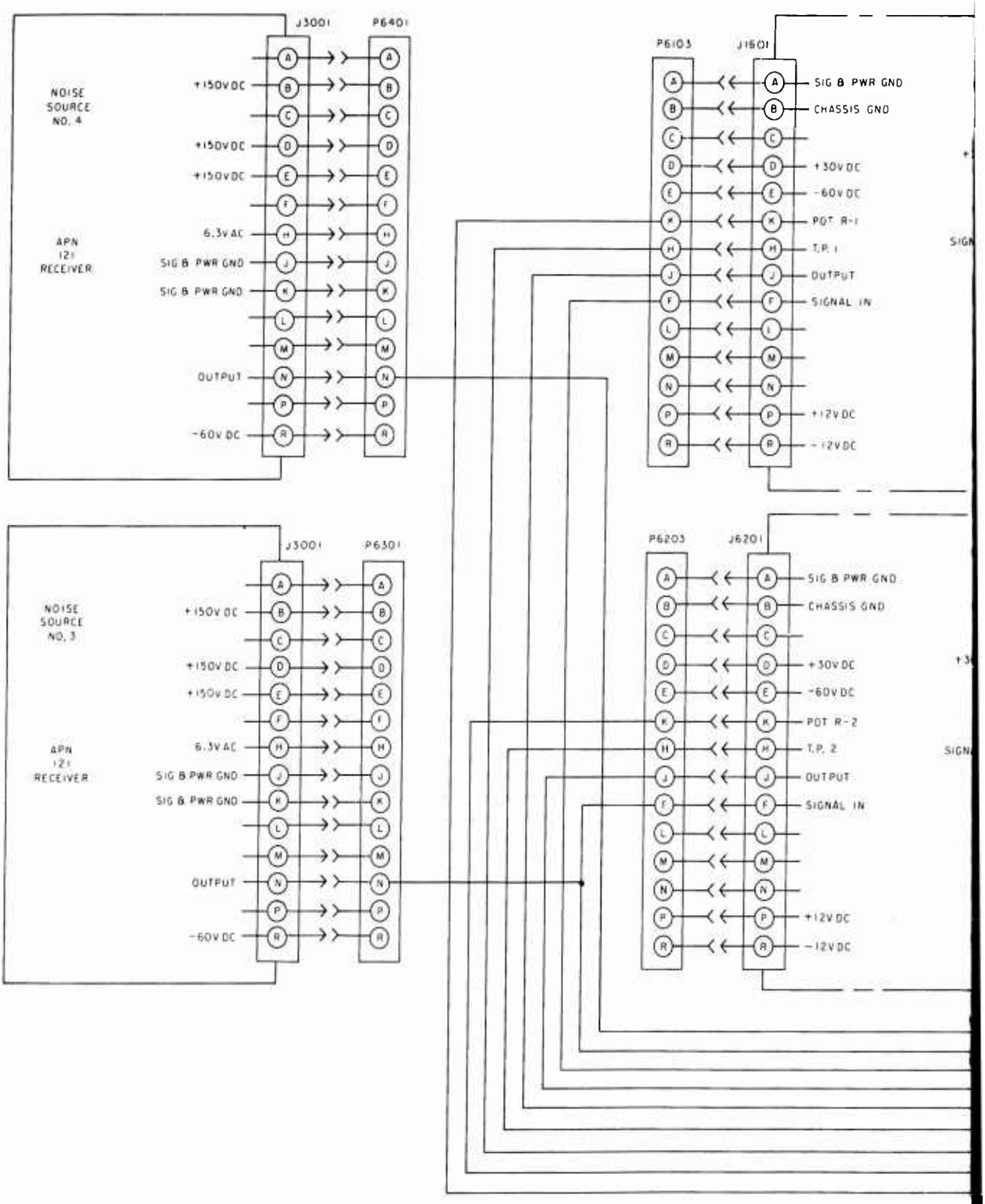




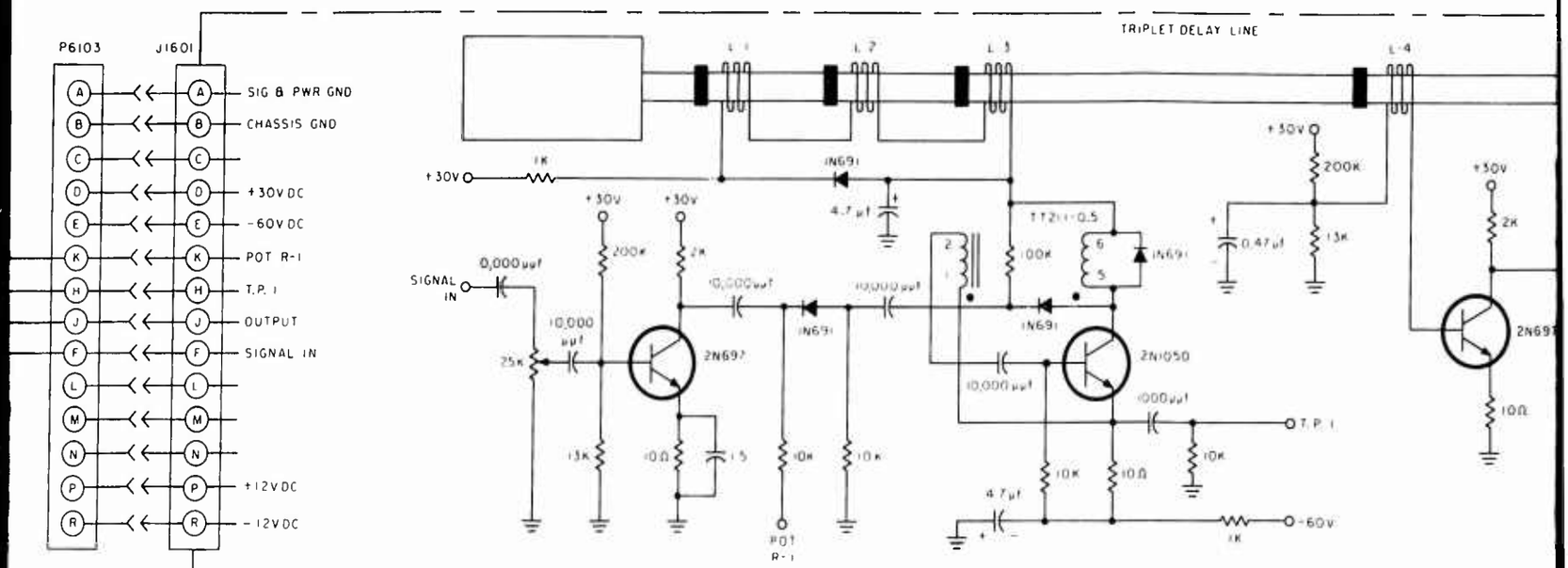
3

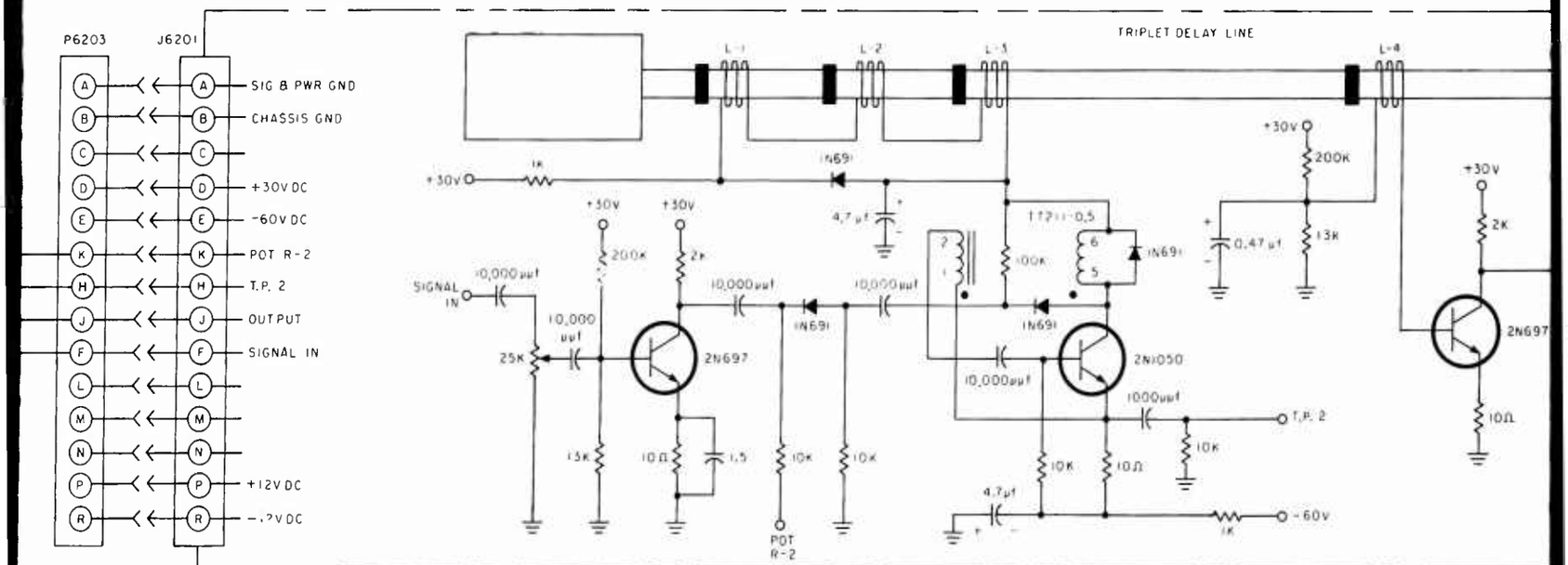
FIGURE 6-3

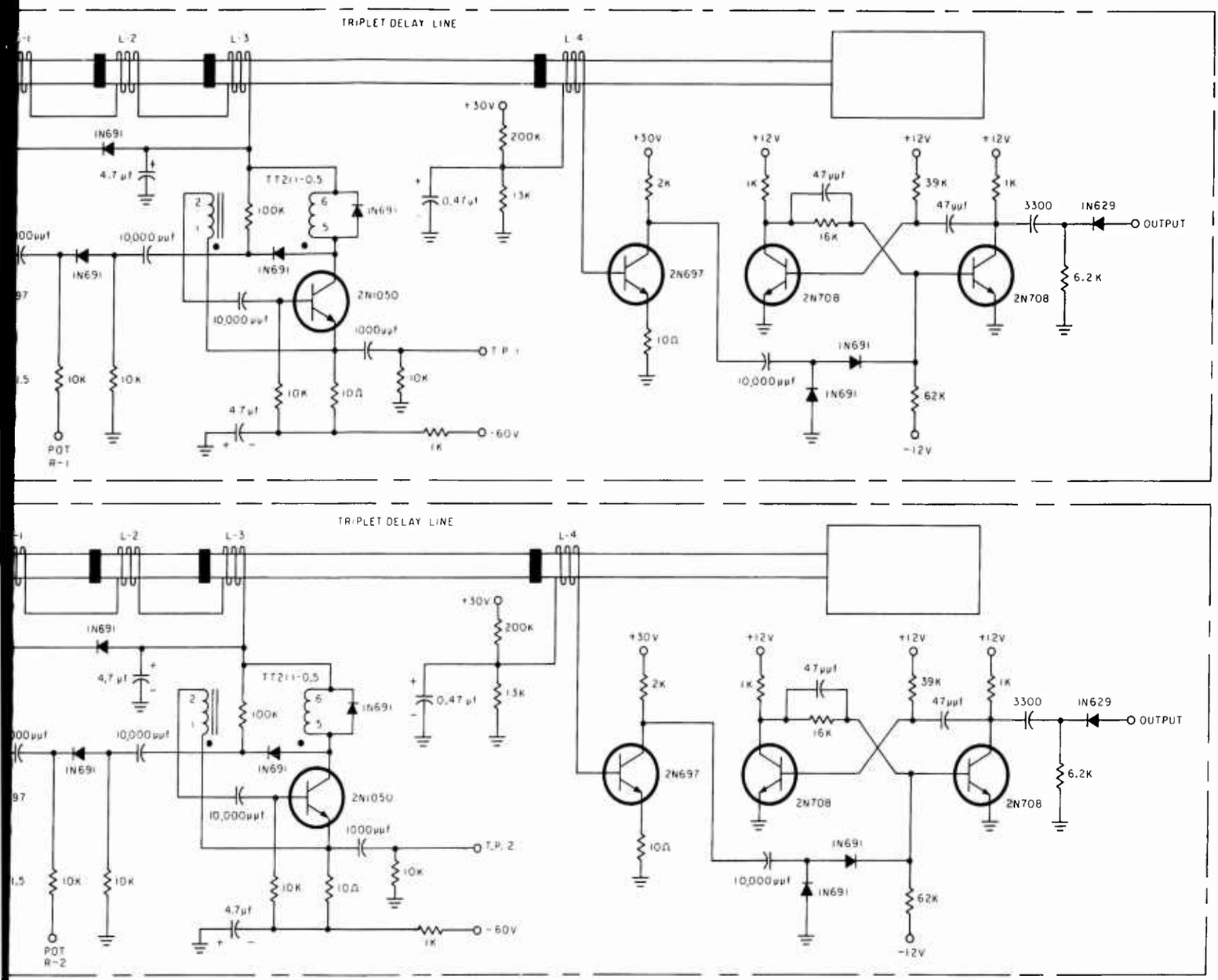
INTERROGATION BACKGROUND NOISE GENERATOR AND SIGNAL CONDITIONER (SHEET 3 OF 3)


J3001
P6401
NOISE SOURCE NO. 4
APN 121 RECEIVER
+15VDC
+15VDC
+15VDC
6.3VAC
SIG B PWR GND
SIG B PWR GND
OUTPUT
-60V DC
P6103
J1601
SIG B PWR GND
CHASSIS GND
+30V DC
-60V DC
POT R-1
T.P. 1
OUTPUT
SIGNAL IN
+12V DC
-12V DC
J3001
P6301
NOISE SOURCE NO. 3
APN 121 RECEIVER
+15V DC
+15V DC
+15V DC
6.3VAC
SIG B PWR GND
SIG B PWR GND
OUTPUT
-60V DC
P6203
J6201
SIG B PWR GND
CHASSIS GND
+30V DC
-60V DC
POT R-2
T.P. 2
OUTPUT
SIGNAL IN
+12V DC
-12V DC


1


P6103
J1601
SIG & PWR GND
CHASSIS GND
+30V DC
-60V DC
POT R-1
T.P. 1
OUTPUT
SIGNAL IN
+12V DC
-12V DC
TRIPLET DELAY LINE
L-1
L-2
L-3
L-4
+30V
1K
IN691
4.7 µf
200K
2K
0,000 µµf
SIGNAL IN
10,000 µµf
25K
2N697
13K
10Ω
1.5
10K
T12(1-0.5
100K
2N1050
1000µµf
T.P. 1
0.47 µf
13K
2K
10Ω
POT R-1
-60V


P6203
J6201
SIG & PWR GND
CHASSIS GND
+30V DC
-60V DC
POT R-2
T.P. 2
OUTPUT
SIGNAL IN
+12V DC
-12V DC
TRIPLET DELAY LINE
L-1
L-2
L-3
L-4
+30V
1K
IN691
4.7 µf
200K
2K
0,000 µµf
SIGNAL IN
10,000 µµf
25K
2N697
13K
10Ω
1.5
10K
T12(1-0.5
100K
2N1050
1000µµf
T.P. 2
0.47 µf
13K
2K
10Ω
POT R-2
-60V



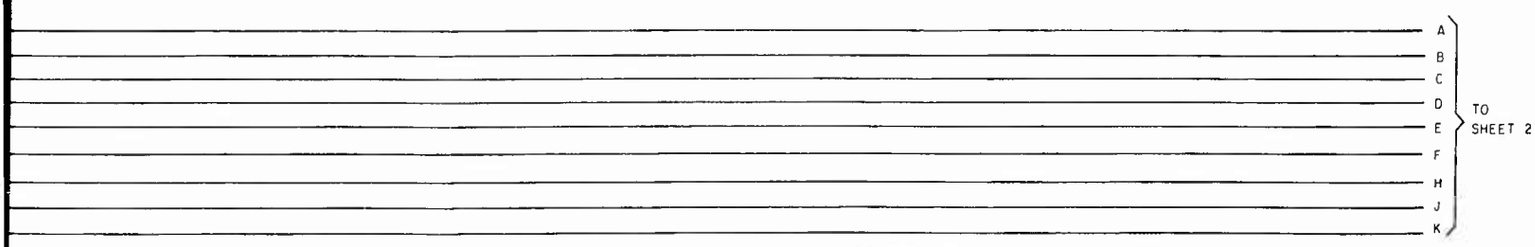
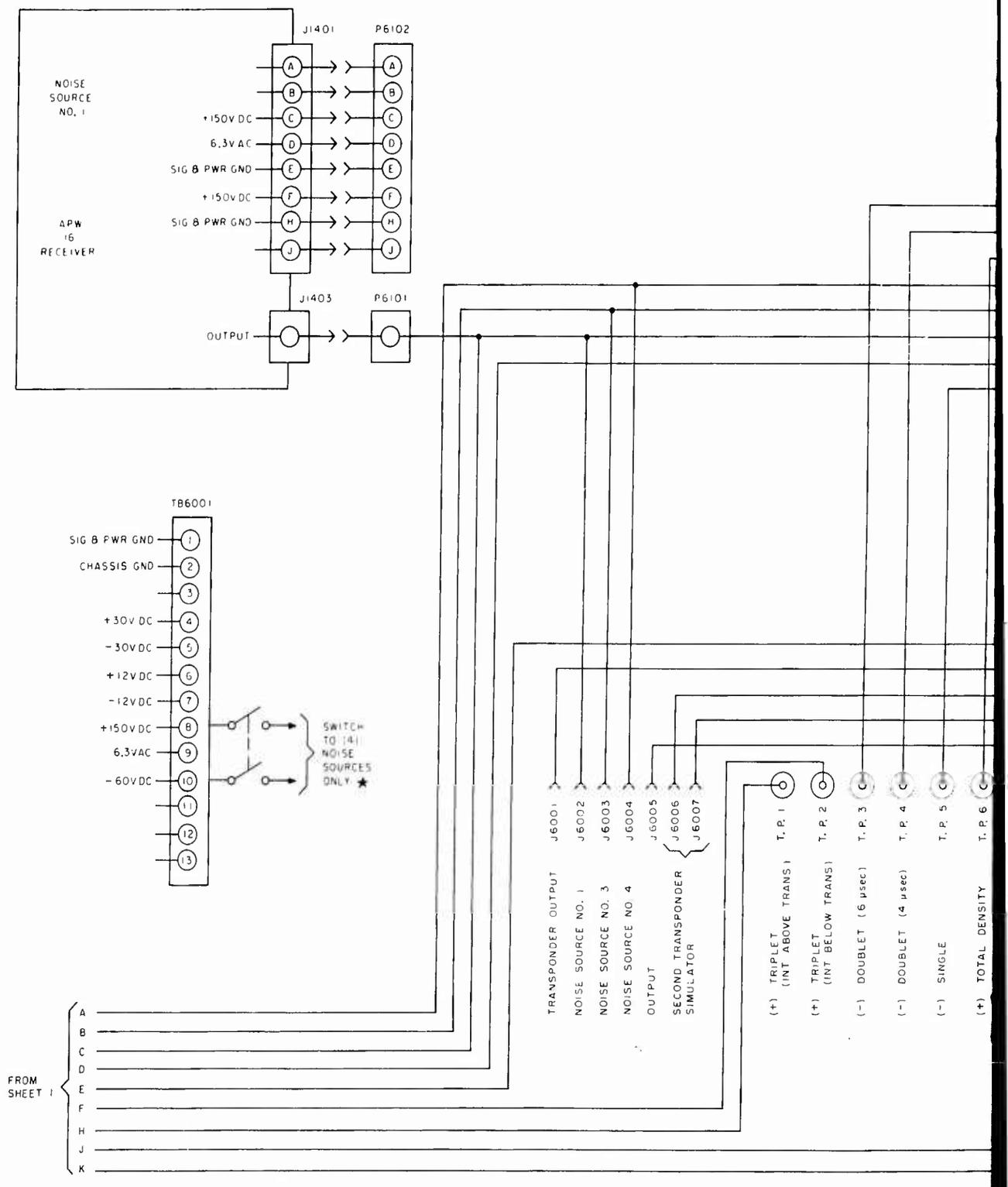


FIGURE 6-4

REPLY BACKGROUND NOISE GENERATOR AND SIGNAL CONDITIONER (SHEET 1 OF 3)

3


J1401
P6102
NOISE SOURCE NO. 1
+150V DC
6.3V AC
SIG & PWR GND
+150V DC
SIG & PWR GND
APW 16 RECEIVER
J1403
P6101
OUTPUT
TB6001
SIG & PWR GND
CHASSIS GND
+30V DC
-30V DC
+12V DC
-12V DC
+150V DC
6.3VAC
-60V DC
SWITCH TO 141 NOISE SOURCES ONLY ★
TRANSPONDER OUTPUT J6001
NOISE SOURCE NO. 1 J6002
NOISE SOURCE NO. 3 J6003
NOISE SOURCE NO 4 J6004
OUTPUT J6005
SECOND TRANSPONDER SIMULATOR J6006 J6007
(+) TRIPLET (INT ABOVE TRANS) T. P. 1
(+) TRIPLET (INT BELOW TRANS) T. P. 2
(-) DOUBLET (6 μsec) T. P. 3
(-) DOUBLET (4 μsec) T. P. 4
(-) SINGLE T. P. 5
(+) TOTAL DENSITY T. P. 6
FROM SHEET 1
A
B
C
D
E
F
H
J
K

1

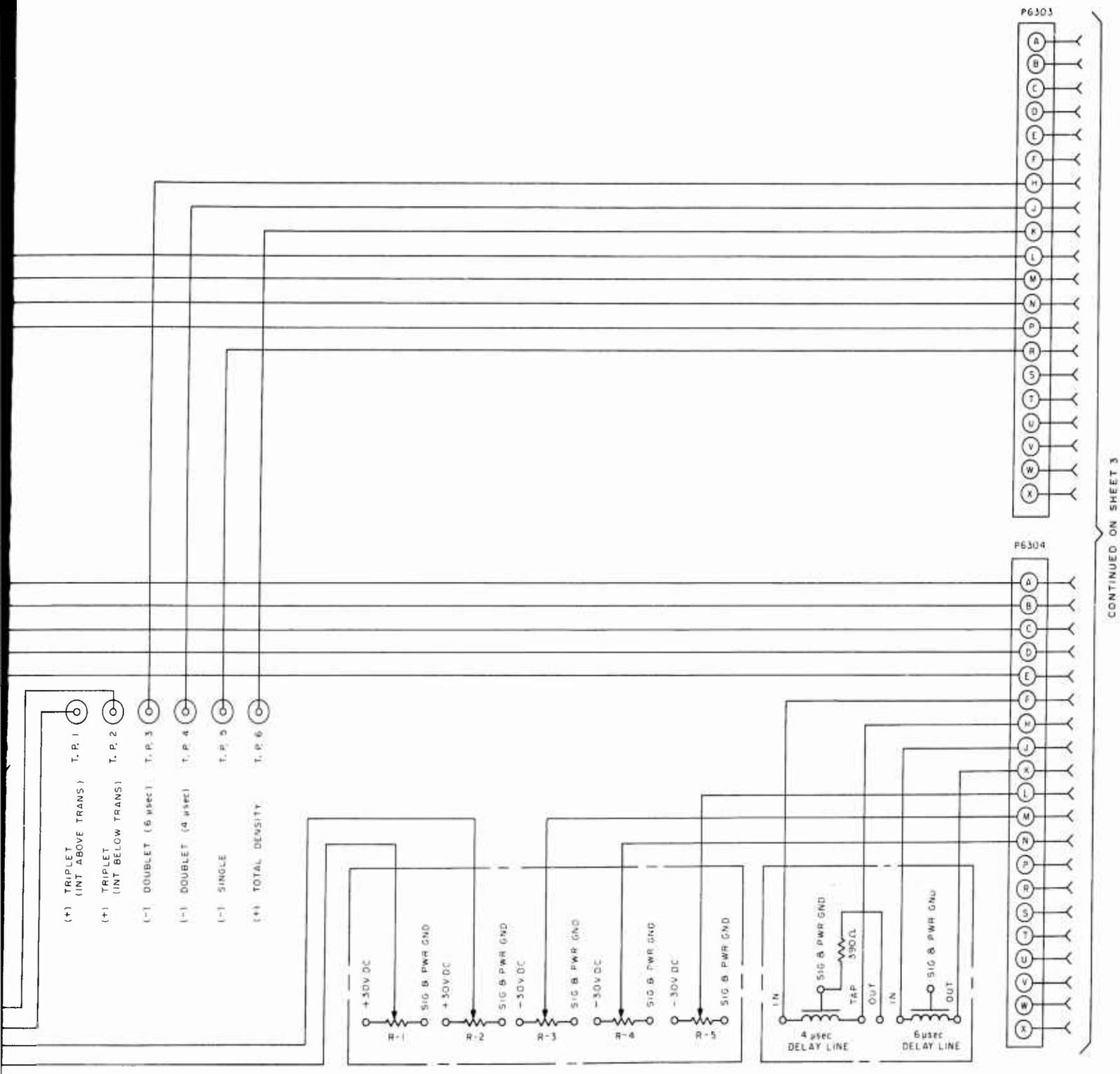


FIGURE 6-4

REPLY BACKGROUND NOISE GENERATOR AND SIGNAL CONDITIONER (SHEET 2 OF 3)

2

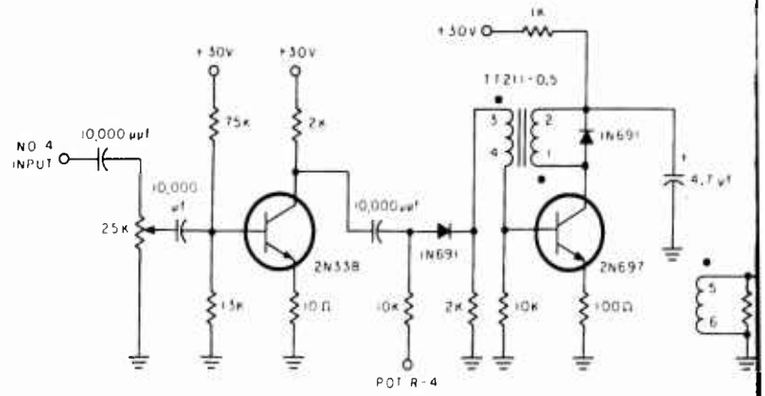
CONTINUED FROM SHEET 2

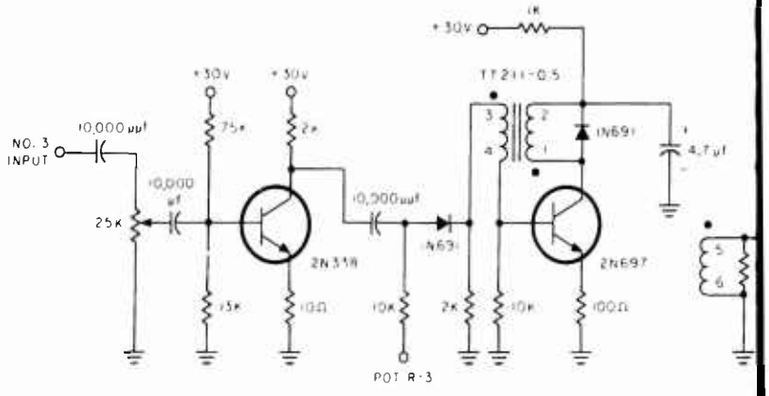
J6301

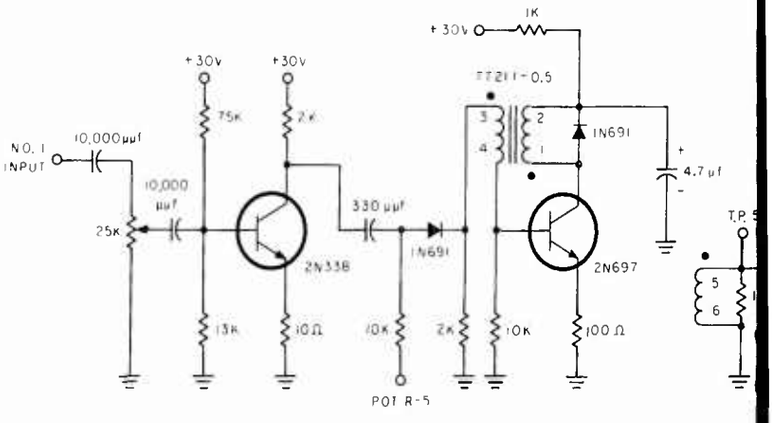
- A — +150V DC
- B — +30V DC
- C — SIG & PWR GND
- D — −30V DC
- E — 6.3V AC
- F — 6.3V AC GND
- H — T.P. 3
- J — T.P. 4
- K — T.P. 6
- L — NO. 4 INPUT
- M — NO. 3 INPUT
- N — NO. 1 INPUT
- P — NO. 2 DELAYED NOISE TRIPLET
- R — T.P. 5
- S
- T
- U
- V
- W
- X

J6302

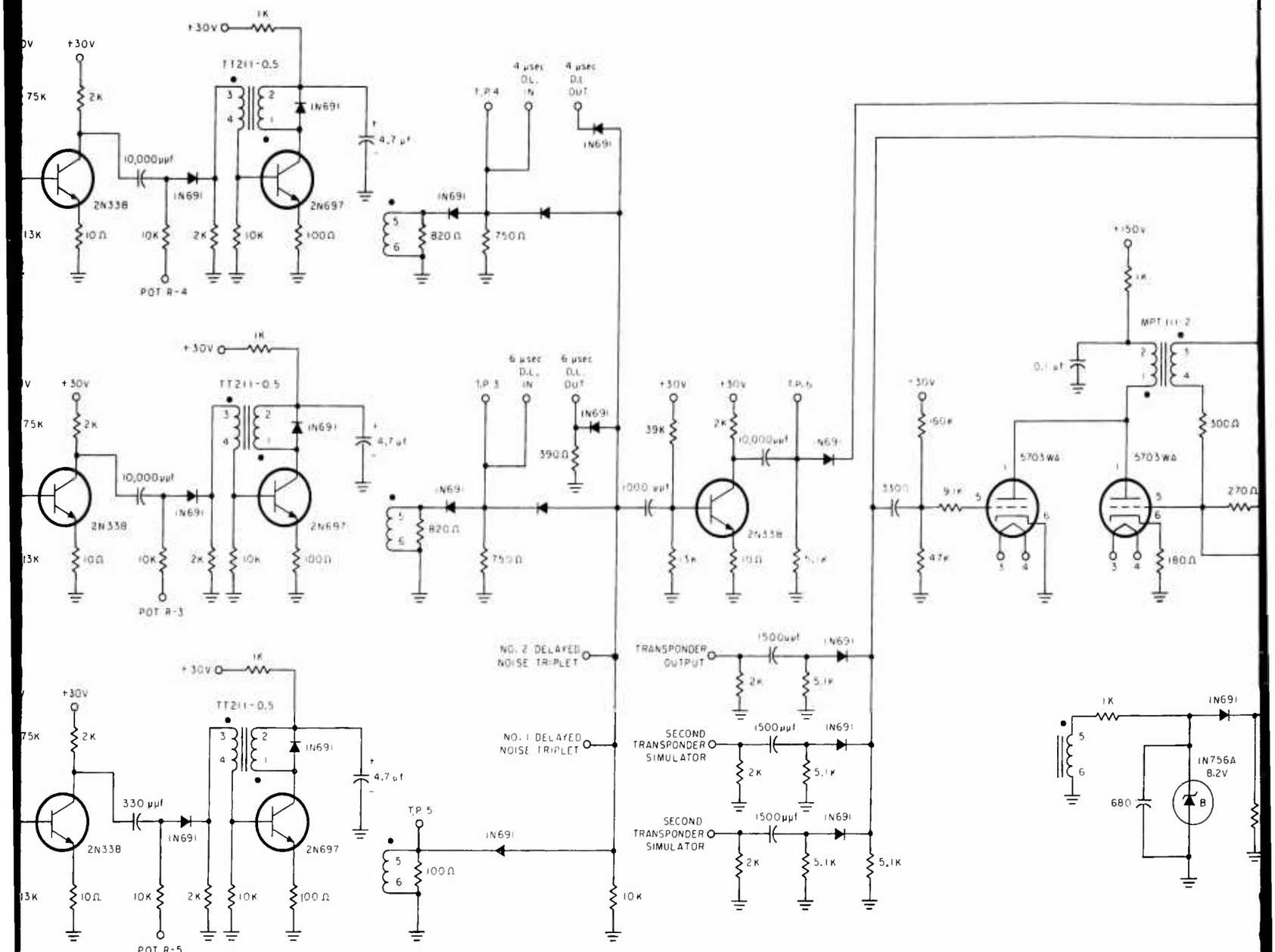
- A — NO. 1 DELAYED NOISE TRIPLET
- B — TRANSPONDER OUTPUT
- C — 2ND TRANSPONDER SIMULATOR
- D — 2ND TRANSPONDER SIMULATOR
- E — REPLY SIG & BACK GND NOISE
- F — 4 μsec D.L. IN
- H — 4 μsec D.L. OUT
- J — 6 μsec D.L. IN
- K — 6 μsec D.L. OUT
- L — POT R-5
- M — POT R-3
- N — POT R-4
- P
- R
- S
- T
- U
- V
- W
- X

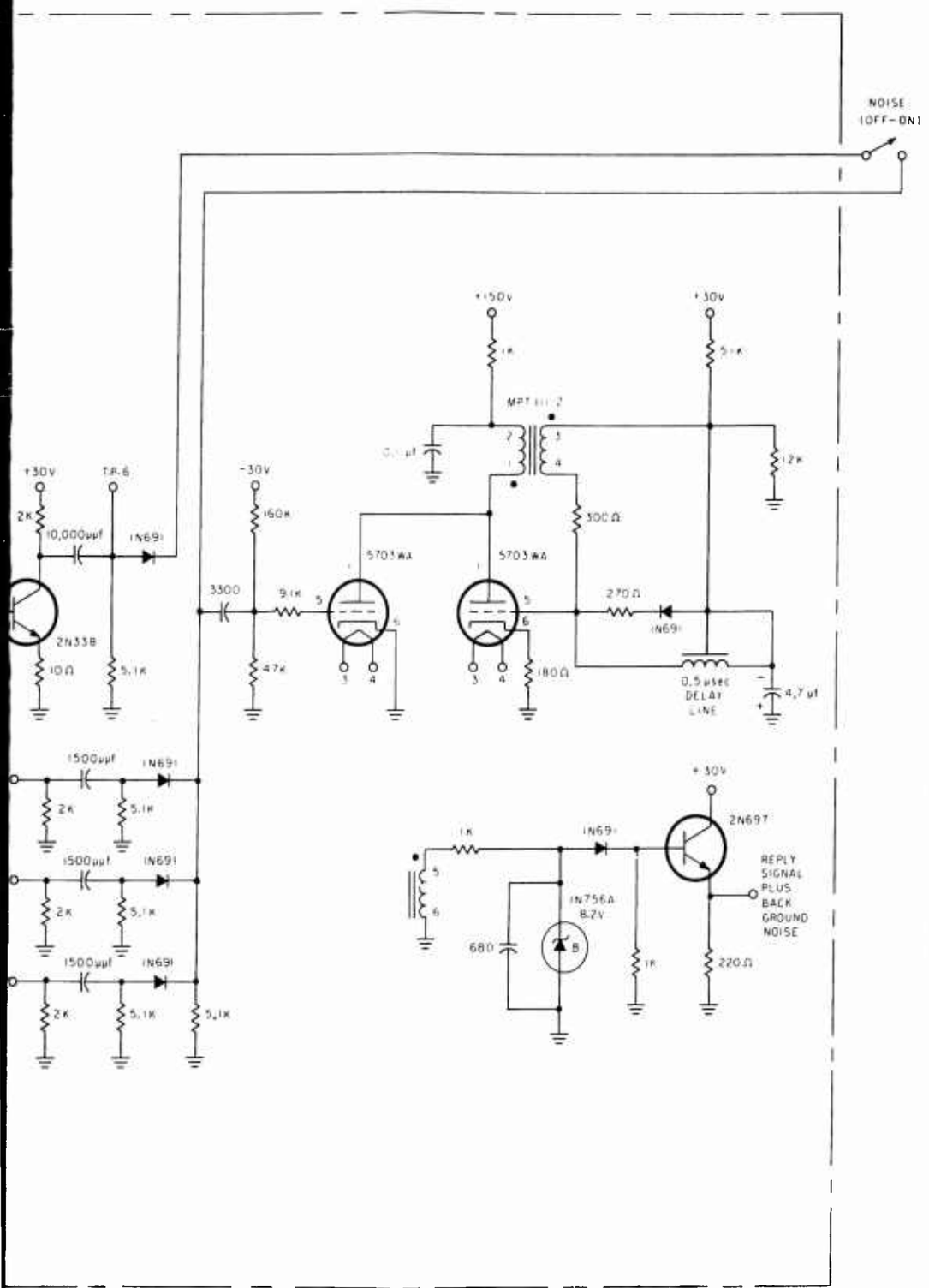






LOGIC CIRCUIT BOARD





3

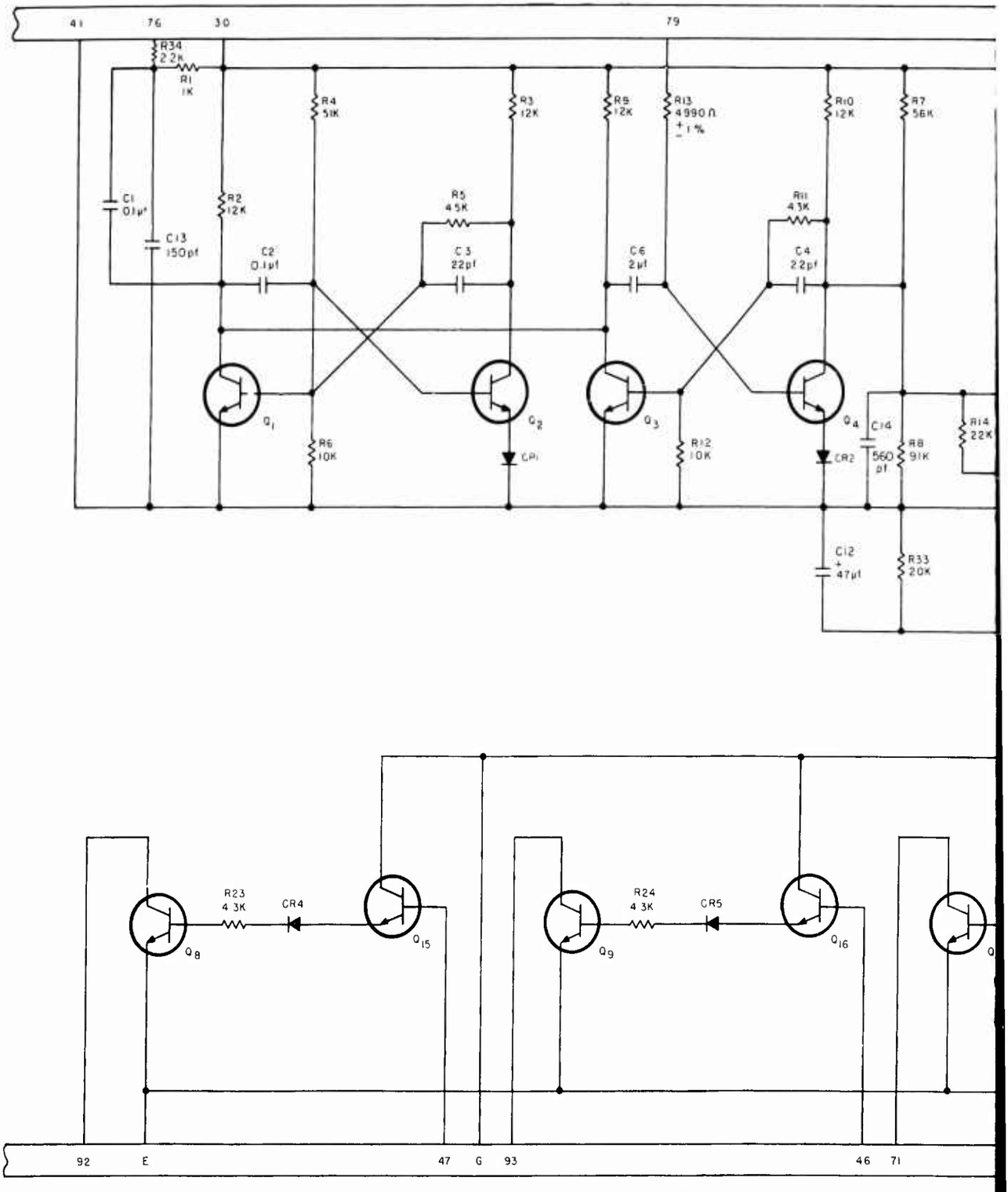
NOTES:

1. POWER INTERCONNECTIONS NOT SHOWN
2. R1 - R5 100K 1W POTS
3. DELAY LINE ASSY NO'S: COIL MOUNT ASSY 4240-00147
   PAD BASE 4240-00143
   PAD COVER 4240-00144
4. APW-16 RECEIVER DRAWING NUMBER 5223-94151
5. APN-121 RECEIVER DRAWING NUMBER 4227-90568
6. ALL TRANSFORMERS PCA ELECTRONICS TYPE AS SHOWN
7. DELAY LINES: 0.5 µsec PCA TYPE DL10000-0.5 RMT
   4 µsec DWG NO 4240-00174
   6 µsec DWG NO. 4240-00174

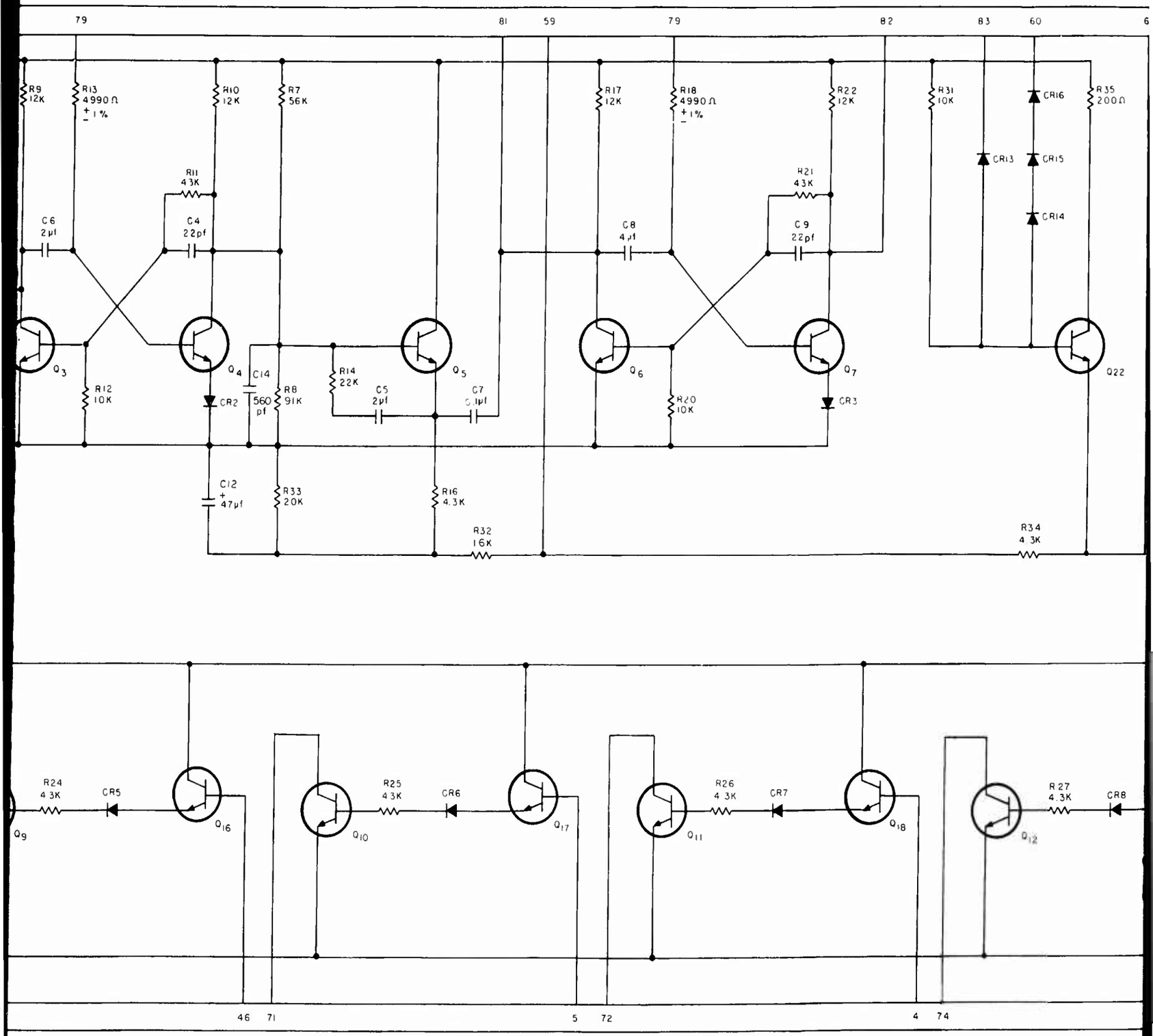
★ +150V AND -60V DC NORMALLY GO TO ALL OTHER CIRCUITS

FIGURE 6-4

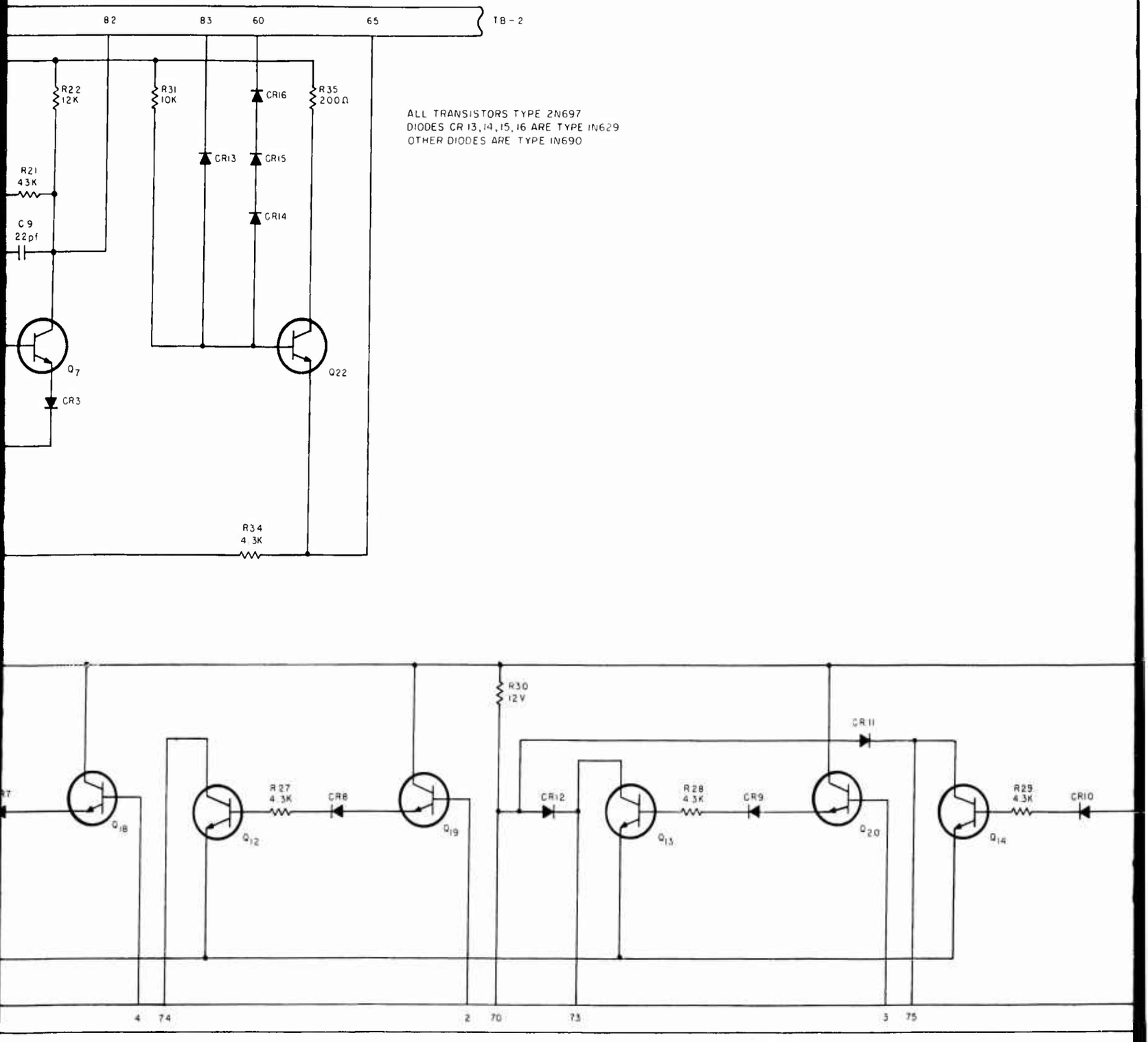
REPLY BACKGROUND NOISE GENERATOR AND SIGNAL CONDITIONER (SHEET 3 OF 3)


41
76
30
79
R34
22K
R1
1K
R4
51K
R3
12K
R9
12K
R13
4990Ω
±1%
R10
12K
R7
56K
C1
0.1μf
R2
12K
C13
150pf
C2
0.1μf
R5
45K
C3
22pf
C6
2μf
R11
43K
C4
22pf
Q1
Q2
Q3
Q4
R6
10K
CR1
R12
10K
CR2
C14
560
pf
R8
91K
R14
22K
C12
+
47μf
R33
20K
R23
4.3K
CR4
Q8
Q15
R24
4.3K
CR5
Q9
Q16
92
E
47
G
93
46
71

1


79
81
59
79
82
83
60
R9 12K
R13 4990Ω ± 1%
R10 12K
R7 56K
R11 43K
C6 2μf
C4 22pf
Q3
Q4
R12 10K
CR2
C14 560 pf
R8 91K
R14 22K
C5 2μf
Q5
C7 0.1μf
C12 + 47μf
R33 20K
R16 4.3K
R32 16K
R17 12K
R18 4990Ω ± 1%
R22 12K
R21 43K
C8 4μf
C9 22pf
Q6
Q7
R20 10K
CR3
R31 10K
CR16
CR13
CR15
CR14
R35 200Ω
Q22
R34 4.3K
R24 4.3K
CR5
Q9
Q16
R25 4.3K
CR6
Q10
Q17
R26 4.3K
CR7
Q11
Q18
R27 4.3K
CR8
Q12
46
71
5
72
4
74

2

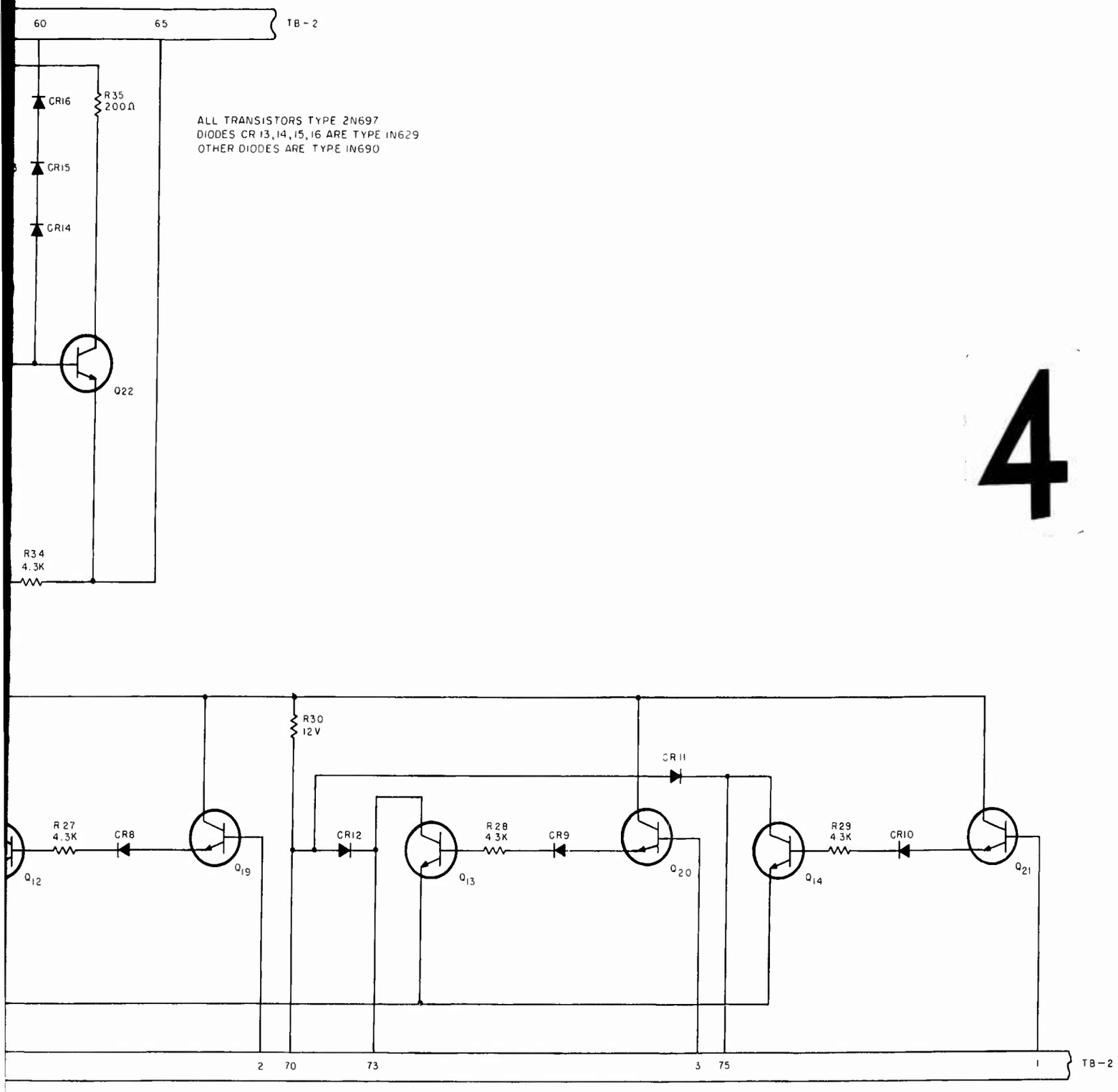


ALL TRANSISTORS TYPE 2N697
DIODES CR 13,14,15,16 ARE TYPE IN629
OTHER DIODES ARE TYPE IN690

FIGURE 6-

ANTENNA SCAN SIMULATOR AND CAS

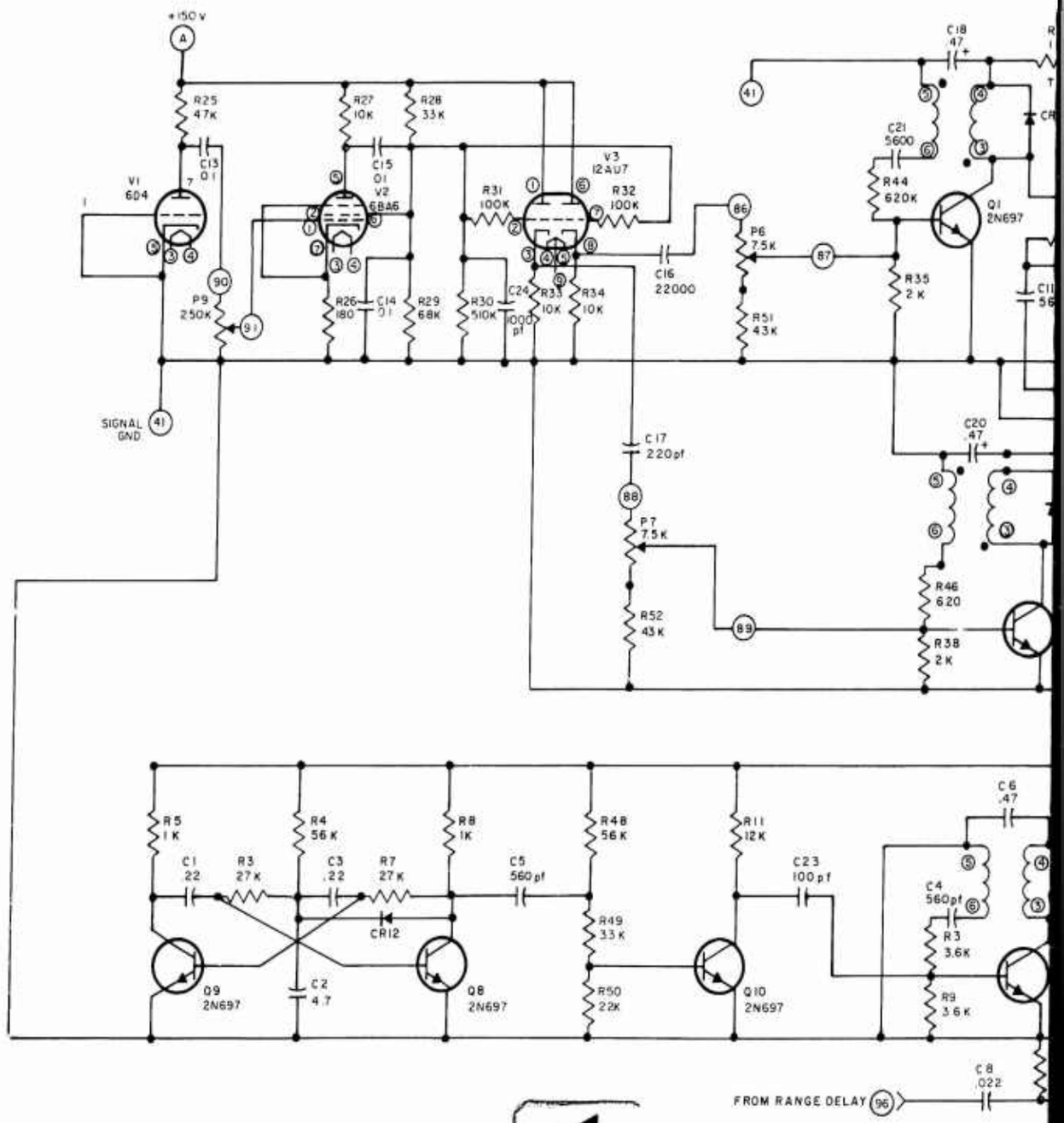
3



4

FIGURE 6-5.

ANTENNA SCAN SIMULATOR AND CAS LIGHT INDICATOR CIRCUIT


+150 V
A
R25 47K
C13 .01
V1 6D4
R27 10K
R28 33K
C15 .01
V2 6BA6
V3 12AU7
R31 100K
R32 100K
C16 22000
P6 7.5K
R51 43K
C18 .47
C21 5600
R44 620K
Q1 2N697
R35 2K
P9 250K
R26 180
C14 .01
R29 68K
R30 510K
C24 1000 pf
R33 10K
R34 10K
SIGNAL GND
C17 220pf
P7 7.5K
R52 43K
C20 .47
R46 620
R38 2K
R5 1K
R4 56K
R8 1K
R48 56K
R11 12K
C1 .22
R3 27K
C3 .22
R7 27K
C5 560pf
C23 100pf
C6 .47
C4 560pf
R3 3.6K
R9 3.6K
CR12
Q9 2N697
C2 4.7
Q8 2N697
R49 33K
R50 22K
Q10 2N697
C8 .022
FROM RANGE DELAY 96

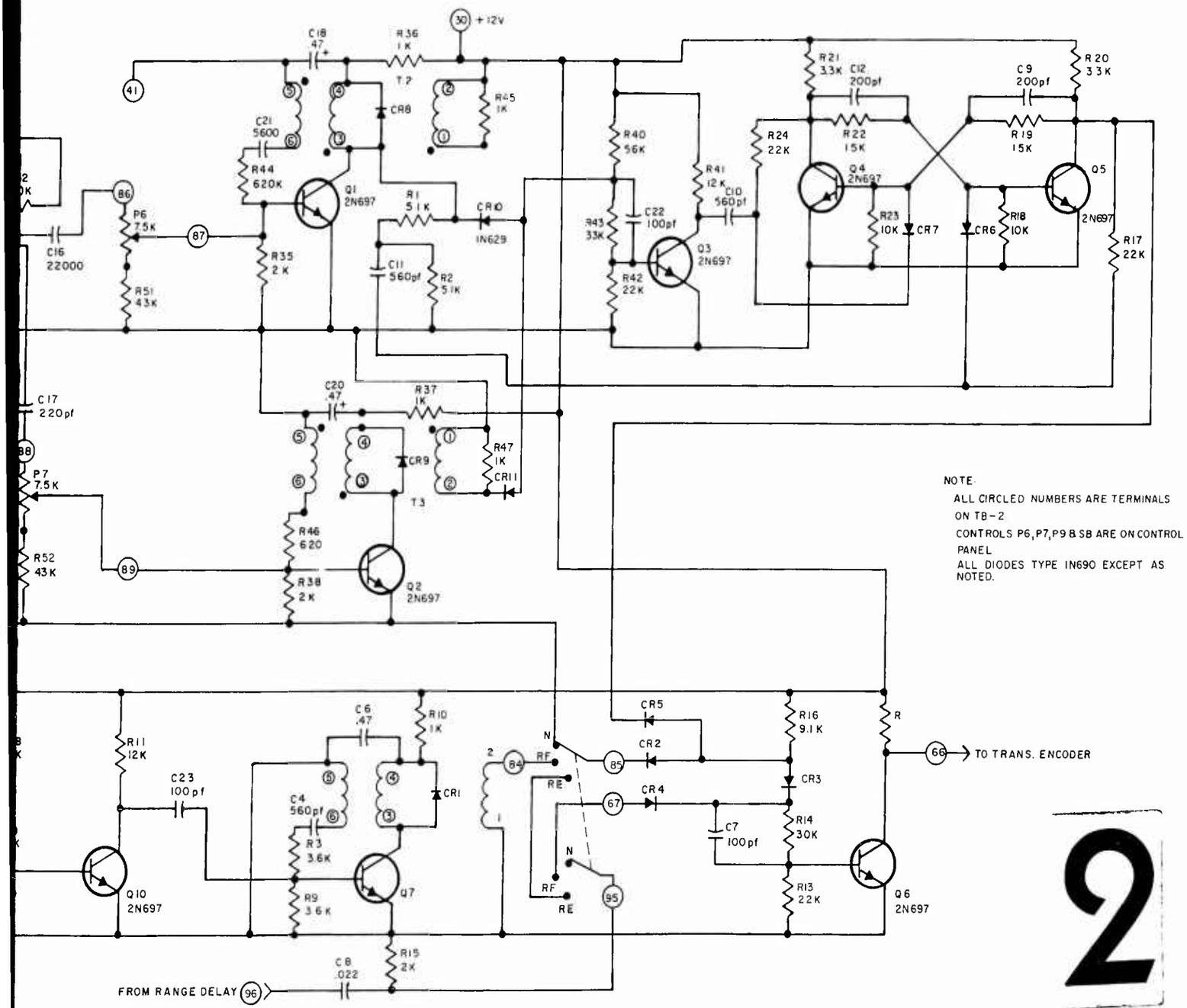
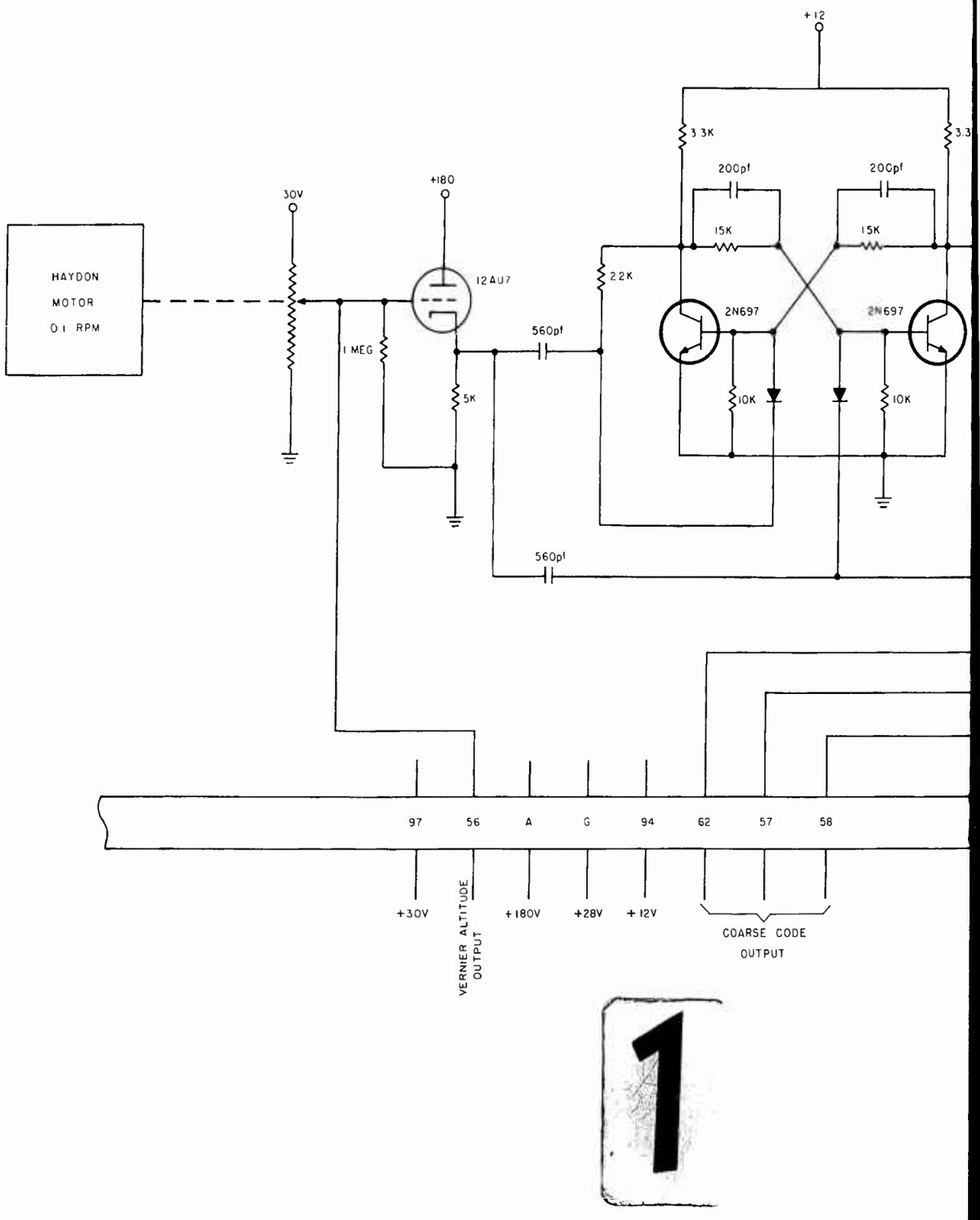


FIGURE 6-6

OVERHEARD REPLY GENERATOR


+12
3.3K
3.3
200pf
200pf
15K
15K
+180
30V
HAYDON
MOTOR
0.1 RPM
12AU7
22K
2N697
2N697
560pf
1 MEG
5K
10K
10K
560pf
97
56
A
G
94
62
57
58
+30V
VERNIER ALTITUDE
OUTPUT
+180V
+28V
+12V
COARSE CODE
OUTPUT

1

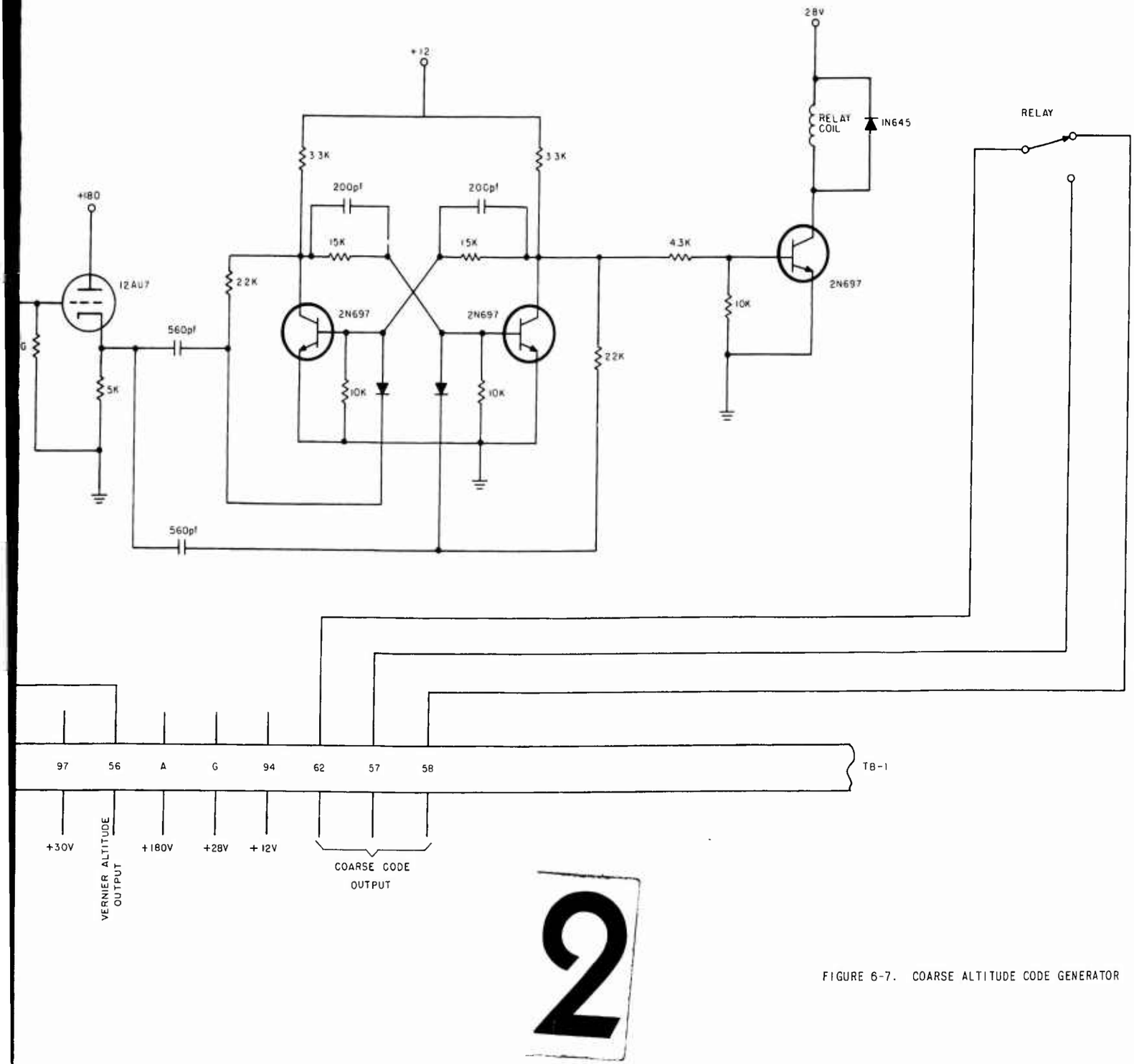


FIGURE 6-7. COARSE ALTITUDE CODE GENERATOR

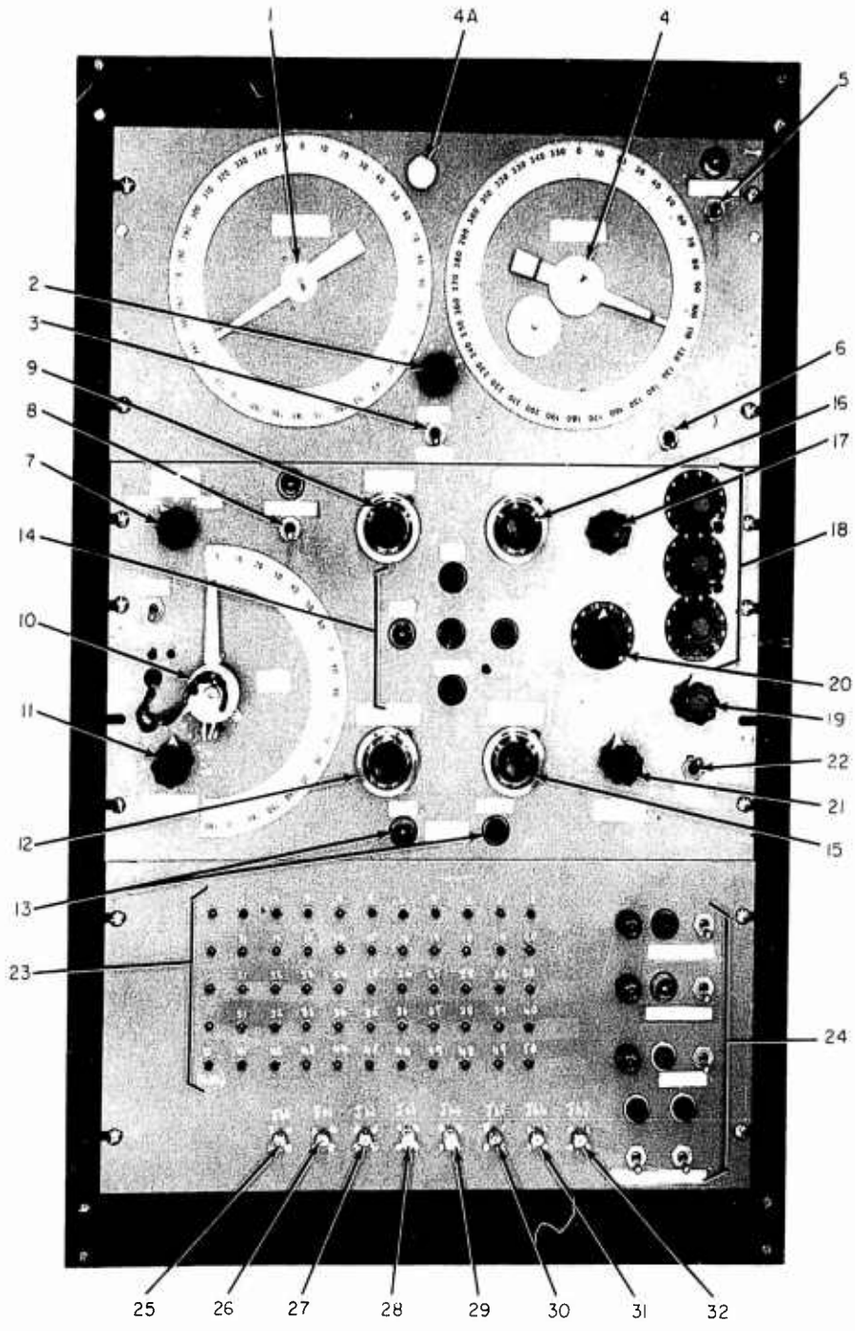


FIGURE 6 8. TEST RACK

16. Transponder Air Speed Control 0-300 Knots

17. Antenna Beam Width Control

18. Overheard Reply Noise Generator Density Controls

The bottom control in this group (P9) controls the output of the noise source and once it is set it can be left alone. The influence of P6 top control and P7 middle control is shown in the following listing:

To Reduce Number Of	P6	P7
Gates	Decrease	Decrease
Pulses	Decrease	Increase
To Increase Number Of	**P6**	**P7**
Gates	Increase	Increase
Pulses	Increase	Decrease

19. Overheard Reply Noise Generator Mode Switch

The positions on this switch have the following meanings:

N	Normal Triggers
RF	Overheard Reply Triggers Added to Normal Triggers
RE	Normal Triggers Interrupted by Random Gates

20. Transponder Altitude Rate Signal

CW rotation produces increasing rate of climb,
CCW rotation produces increasing rate of descent.
Gradient is 0.25v per 1000 feet per minute.

21. Transponder Coarse Altitude Selector Switch

22. Scan Simulator Mode Switch. RF., RE., positions not used

23. Test points associated with number designation of TB-3 on Test Rack Schematic Diagram

24. On-Off Power Switches

25. Transmit Trigger Pulses enter Test Rack from Interrogator Encoder

26., 27. Second Transponder Simulator Output Pulses. Not used.

28. Reply Video Input to Second Transponder Simulator. Not used.

29. Transmit Trigger Input to Second Transponder Simulator. Not used.

30. Video Input from Interrogator Encoder to Transponder Decoder.

31. Delayed Transponder Reply Triggers Plus Overheard Reply Triggers.

32. Delayed Transponder Reply Triggers into Test Rack from Rutherford Range Delay Simulator.

B. ALIGNMENT

Instructions for alignment of the breadboard and test equipment, where adjustments are provided, are included here in the event that the adjustment is inadvertently changed or that some readjustment is required as the equipment ages. The instructions that follow for alignment of each circuit should be followed in the order given. In the cases where there are several adjustments made on one card the adjustments should be repeated until the desired result is obtained. This is necessary because some effects are influenced by more than one variable.

1. Test Equipment-Antenna Scan Simulator

Alignment of the antenna scan simulator is easily done by adjusting the bearing simulator synchro housing such that the synchro null lies at the center of the beam i.e., at T_0 as is shown in figure 6-9. With this adjustment made as previously described the bearing pointer is set at 0 degrees on the scale and locked to the case. Thereafter, any rotation of the case will move the 0-degree null (and pointer) away from the beam center as desired for the purpose of setting relative bearing.

2. Breadboard Equipment

1100 Pulse and Gate Generator - Mixer Amplifier

R5 System Repetition Rate Adjustment (200 cps); Monitor J1101-M

1300 Vernier Coder

R14 Sweep Slope Adjustment; monitor J1301-S for a delayed pulse 40 usec from a pulse input at J1301-L when +30 volts is applied to J1301-P.

R25 Zero Set Adjustment; monitor J1301-S for a delayed pulse 20 usec from a pulse input at J1301-L when J1301-P is grounded.

R26 4-usec Adjustment; monitor J1301-R to obtain a pulse 4 usec prior to the pulse output of J1301-S for any voltage value (0 to 30 volts) input on J1301-P with a pulse input on J1301-L with no Maneuver Command from the computer.

R27 6-usec Adjustment; repeat R26 test with Maneuver Command input from computer on J1301-N to obtain a 6-usec spacing.

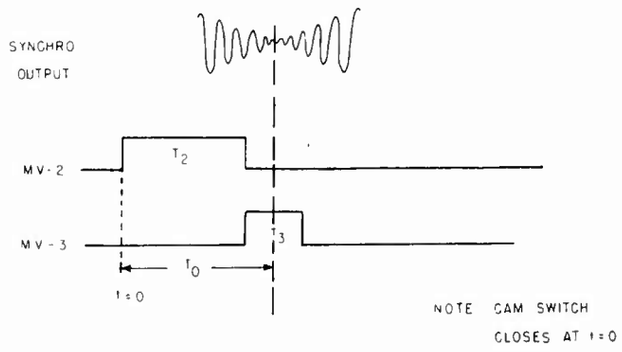


FIGURE 6 9. SCAN SIMULATOR ALIGNMENT

2500 A&B — North and East Velocity Decoders

R25 & 39	Balance Control Adjustments; ground circuit between R-7 and C-5 and adjust R25 and R39 to give zero volts at J2501-M and -N respectively.
R14	Slope Adjustment; with pulse inputs at J2501-K and -L at 30-usec spacing adjust R14 to give +12 volts and -12 volts at J2501-M and -N respectively (See Note 1)
R24	Zero Set Adjustment; with pulse inputs at J2501-K and L at 10-usec spacing adjust R24 to give +12 volts and -12 volts at J2501-M and -N respectively (see Note 1). (Note 1: Repetition rate of pulse inputs to be 200 cps (5000 usec) with positive and negative reset pulses of 7-usec duration at J2501-S and -R respectively appearing a minimum of 28 usec prior to the pulse input at J2501-K).

2600 — Blanking Logic

R3	Range Blanking Gate Width Adjustment; with a pulse input at J2601-R set R3 to give a 8-usec gate at J2601-J.
R51	Maximum Range Gate Adjustment; with a pulse input at J2601-M set R51 to give a gate (X+28 usec long) at the collector of Q16, where X = 12.4 (desired max. range), in microseconds.

2700 — Blanking Sweep Generator

R25	Provide a jumper from collector of Q4 to ground. Adjust R-25 for a zero volts dc on pin X of J2701. Remove jumper.
R24	Monitor the pulse output at J2801-M. Set the reply delay at short range and adjust R-24 such that the pulse at J2801-M precedes the reply trigger by 4-usec.
R14	Repeat the procedure above except that the range delay should be set at about 200 usec and adjustment is made with R-14.

2800 — Range Sweep Generator

R25	Balance Control Adjustment; with circuit grounded between R-7 and C-5 set R26 to obtain zero volts at J2801-J.
R14	Slope Adjustment; with pulse inputs at J2801-P and -L of 208-usec spacing adjust R14 to give +18 volts at J2801-J. (See Note 2)

R24 Zero Set Adjustment; with pulse inputs at J2801-P and -L of 40-usec spacing, adjust R24 such that the voltage at J2801-J crosses zero volts 28 usec after the pulse inputs at J2801-P. (See note 2)

(Note 2: Repetition rate of pulse inputs to be 200 cps (5000 usec) with positive reset pulse of 7-usec duration at J2801-R appearing a minimum of 36 usec prior to the pulse input at J2801-P).

R35 Blanking Pulse Zero Set; remove and ground lead to J2801-N, with pulse inputs at J2801-P and -L of spacing from 40 to 180 usec, adjust R35 to obtain a pulse output at J2801-M, 27 usec after the pulse input at J2801-P.

3200 A&B North and East Velocity Coders

R17 Sweep Slope Adjustment; adjust R17 and monitor J3201-S for a delayed pulse 30 usec from a pulse input at J3201-L when +30 volts is applied to J3201-P.

R26 Zero Set Adjustment; adjust R26 and monitor J3201-S for a delayed pulse 10 usec from a pulse input at J3201-L when J3201-P is grounded.

R29 4-usec Adjustment; adjust R-29 and monitor J3201-R to obtain a pulse 4 usec prior to the pulse output of J3201-S for any voltage (0 to + 30 volts) input on J3201-P when +12 volts is applied to J3201-N.

R27 6-usec Adjustment; repeat as previously described but with R-27 and with lead to J3201-N open to obtain a 6-usec spacing.

4300 Band Decoder

R17 30-usec Gate Adjustment; lift and apply to Q-2 end of C-8 a negative trigger pulse, monitor the collector of Q-6 and adjust R-17 to obtain a 30-usec pulse.

4400 Two-Pulse Delay Generator

R17 Slope Adjustment; monitor emitter of Q-7 to obtain a 20-volt sweep in 50 usec with an input pulse to J4401-K. (R26 may require adjustment to obtain 50 usec)

R26 20-usec Adjustment; adjust R26 and monitor J4401-L to obtain a pulse 20 usec after the input pulse on J4401-K.

R60 40-usec Adjustment; adjust R60 and monitor J4401-M to obtain a pulse 40 usec after the input pulse on J4401-K.

4500 Three-Pulse Delay Generator

R17 Slope Adjustment; monitor emitter of Q-7 to obtain a 20-volt sweep in 50 usec with an input pulse to J4501-K. (Note: R79 may require adjustment to obtain 50 usec.)

R78 Mid-Pulse Adjustment; monitor J4501-R with +30 volts applied to J4501-M adjust R-17 and R78 for a pulse 40 usec after the pulse applied to J4501-K. Apply 0 volts to J4501-M and adjust R78 for a pulse 20 usec after the pulse applied to J4501-K.

R79 Late-Pulse Adjustment; monitor J4501-P. Apply 0 volts to J4501-M and adjust R79 for a pulse 22.4 usec after the pulse applied to J4501-K.

R80 Early-Pulse Adjustment; monitor J4501-S. Apply 0 volts to J4501-M and adjust R80 for a pulse 17.6 usec after the pulse applied to J4501-K.

A-3 Relative Bearing Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v, 400 cps to transmitter rotor red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low) leads. This position is 0 degrees (north).

Alignment Procedure for Differential

Connect differential to transmitter as shown with transmitter at 0 degrees. Rotate differential housing for a null across rotor black and yellow (low) leads. Rotation of the transmitter rotor shaft cw shall produce an increasing in-phase voltage across the differential rotor black and yellow (low) leads.

Alignment Procedure for Resolver Transmitter

Apply 26v, 400 cps to resolver transmitter rotor white-red and white-black (low) leads with white-yellow and white-black leads connected together. Rotate rotor for a null across red and black (low) leads of stator. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and red (low) leads of stator. This position is 0 degrees for the antenna train angle.

Alignment Procedure for Resolver

Connect resolver transmitter to resolver as shown with transmitter at 0 degrees. Rotate resolver housing for a null across rotor black and red (low) leads. Rotation of resolver transmitter shaft cw shall produce an increasing out-of-phase voltage across resolver rotor black and red (low) leads.

Alignment Procedure for Sine-Cosine Pot

With transmitter at 0 degrees connect 3 volts dc across 1 and 3 (low). Connect a d-c voltmeter across 1 and 4. Rotate potentiometer housing for a null, connect low side of voltmeter to 3 and measure the following voltages: 5 to 3, 8 to 3, 6 to 3, 7 to 3, which shall be 15v dc and 2 to 3 which shall be a null.

A-4 Magnetic Bearing Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v, 400 cps to red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads of stator. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low) leads. This position is 0 degrees, $(\theta' + \theta_c + \alpha) = 0^{\circ}$

Alignment Procedure for Sine-Cosine Pot P1

With transmitter at 0 degrees connect 3 volts dc across 1 and 3 (low) connect a dc voltmeter across 1 and 2. Rotate potentiometer housing for a null. Connect low side of voltmeter to 3 and measure the following voltages: 5 to 3, 7 to 3, 8 to 3, 6 to 3. which shall be 1.5v, while 4 to 3 shall be a null.

Alignment Procedure for Sine-Cosine Pot P2

The potentiometer shafts of P1 and P2 should be aligned by the vendor. To check alignment repeat the same test for P1 as previously described.

Operational Amplifiers

All of the operational amplifiers are nulled by the following procedure. Special conditions for the particular amplifier being adjusted are as follows:

Test Conditions

A-7 Velocity Integrators

Short A-7-T and V to Ground. Open A-7 P. Add 100K ohm resistor across each 0.33 μf capacitor. Proceed with adjustments.

A-8 Normal Velocity Adder

Open terminals P8-V, X, T. Short 1-megohm resistor from P8-V to ground. Proceed with null adjustments.

A-9 Radial Velocity Adder

Open terminals P9-V, X, T. Short 1-megohm resistor from P9-V to ground. Proceed with null adjustments.

A-10 Range Adder

Open terminal P10-T, short circuit 820-ohm resistor of input bias circuit on A-10 card. Proceed with null adjustments.

Nulling Procedure

Place a one-millivolt meter from the amplifier output terminal to the summing junction. This meter input must be isolated from ground. Place another millivolt meter from the output terminal of the amplifier to ground. Alternately adjust the offset potentiometer at the rear of the card and the current null potentiometer located at the center of the card to produce readings as near zero as possible on both meters.

A-24 Heading Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v, 400 cps to rotor of transmitter red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads. Rotation of rotor shaft cw shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low), this position is 0 degrees (north).

Alignment Procedure for Control Transformer (CT)

Connect transmitter to CT as shown. With transmitter at 0 degrees rotate housing of CT for a null across CT rotor leads white-red and white-black (low). CW rotation of transmitter shaft shall produce an increasing in-phase voltage across white-red and white-black (low) leads.

Alignment Procedure for Sine-Cosine Pot

Disconnect all leads from terminal 3 on potentiometer. Connect 3v dc across 1 and 3 (low) (transmitter at 0 degrees). Rotate potentiometer housing for a null across 1 and 2. Connect low side of voltmeter to 3 and measure the following voltages: 5 to 3, 6 to 3, 8 to 3, 7 to 3, which shall be 1.5v while 4 to 3 shall be a null. Reconnect wires to terminal 3. The pot and switch shafts are aligned by the vendor. To check alignment, connect an ohmmeter across 1 and 2 of S1 with the 0-degree condition previously described. If there is continuity, no more than three turns ccw of the slotted journal of the gear train shall break continuity. If there is no continuity, no more than four turns cw shall produce continuity. With 3v dc across 1 and 5 (low) of pot, rotate slotted journal ccw for a null across 6 to 1. Check alignment of S2 the same as S1 previously described. Rotate slotted journal cw for a null across 1 and 2 of pot. The CT a-c voltage F to A (low) shall be at a null. Rotation of the slotted journal ccw shall produce an out-of-phase voltage across CT output F and A (low).

A25 Altitude Servo

Note: All rotations viewed from shaft end

Alignment Procedure for Transmitter

Apply 26v, 400 cps to transmitter rotor red and black (low) leads. Rotate rotor for a null across black and yellow (low) leads of stator. CW rotation of the rotor shall produce an increasing out-of-phase voltage across black and yellow (low) leads of stator. Rotate rotor back to a null across black and yellow (low) leads. This position is 0 degrees (zero altitude).

Alignment Procedure for Potentiometer P1

For zero altitude, wiper 2 must be 250.2 degrees cw from terminal 3. To accomplish this the set-up in figure 6-10a is used. Select a value of R_1 = 10K. Then R2 will be

$$R2 = 10K \times \frac{356.4}{250.2} - 10K$$

$$R2 = 4244\Omega$$

Connect R1 and R2 as shown in figure 6-10a. Rotate housing of P1 for a null on voltmeter. Resistors should be $\pm$ 1% or less.

Alignment Procedure for P2

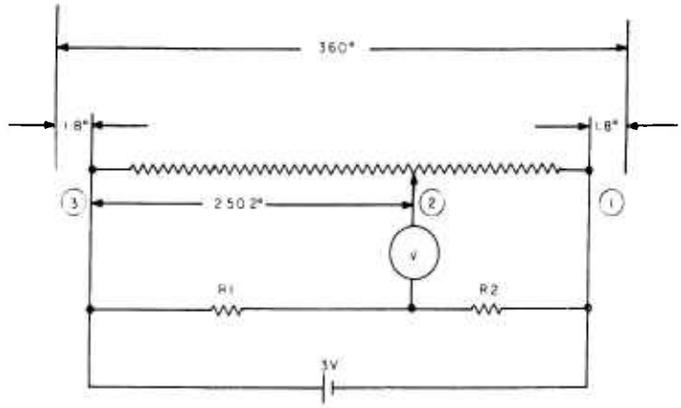
The wiper of P2 shall be 180 degrees away from wiper of P1. This should be done by the vendor. To check it use the set up in figure 6-10a. The wiper will be at 70.2 degrees; therefore

$$R2 = 10K \times \frac{356.4}{70.2} - 10K$$

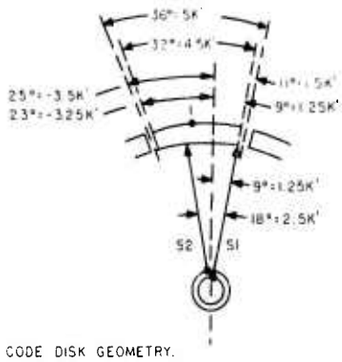
$$R2 = 40767\Omega$$

Alignment Procedure for Code Wheel Commutator

From the geometry of figure 6-10b, it is seen that for zero altitude, brush S1 is at the edge of segment 1 of the commutator. Set transmitter for 0 degrees (zero altitude). Connect an ohmmeter (on the R x 100 scale) across 1 and S1. Rotate code wheel housing ccw until continuity just exists. There should be continuity from 1 to S2. If there is not, rotate housing ccw until continuity just disappears across 1 and S1.



A TEST CIRCUIT FOR ALTITUDE POTENTIOMETERS



B ALTITUDE CODE DISK GEOMETRY.

FIGURE 6-10. ALTITUDE SERVO ALIGNMENT